Exhibit 13

Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 8,787,060

Issued: July 22, 2014

Filed: November 3, 2011

Inventor: Hyun Lee

Title: Method and Apparatus for Optimizing Driver Load in a Memory Package

Inter Partes Review No. IPR2022-01428

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,787,060

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1011	U.S. Patent Application Publication No. 2008/0025137 to Rajan *et al.* (published Jan. 31, 2008)
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1013	U.S. Patent Application Publication No. 2006/0259678 to Gervasi (published Nov. 16, 2006)
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1036	[omitted]
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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory package, comprising:
1.b	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
1.c	a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
1.d.1	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
1.d.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
1.e.1	a control die comprising
1.e.2	at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals,
1.e.3	and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal,
1.e.4	the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.
2	The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.
3	The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.
4.a	The memory package of claim 3, wherein the control signals include command/address signals and
4.b	wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.

Ref. #	Listing of Challenged Claims
5	The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.
6.a	The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising:
6.b	third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.
7.a	The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit,
7.b	the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.
8.a	The memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals,
8.b.1	wherein the control die is configurable to operate in any one of a first mode and a second mode, and wherein:
8.b.2	in the first mode, the control die receives the data path control signals from the one or more external devices; and
8.b.3	in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.
9	The memory package of claim 1, wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address.

Ref. #	Listing of Challenged Claims
10	The memory package of claim 1, wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies.
11.a	A memory package, comprising:
11.b	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;
11.c	a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;
11.d.1	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
11.d.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
11.e.1	a control die comprising
11.e.2	at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals,
11.e.3	at least a second data conduit between the second die interconnect and the first terminal, and
11.e.4	chip select conduits for providing chip select signals to respective array dies;
11.e.5	wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.
12	The memory package of claim 11, wherein the chip select conduits pass through the control die.
13	The memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies.

Ref. #	Listing of Challenged Claims
14	The memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.
15.a	The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and
15.b	wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.
16	The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.
17	The memory package of claim 11, wherein the control circuit controls the respective states of the fist data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.
18	The memory package of claim 16, wherein the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal.
19.a	The memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and
19.b	wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.
20.a.1	A method for optimizing load in a memory package comprising
20.b.1	a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die,
20.b.2	at least a first die interconnect and a second die interconnect,
20.b.3	a control die, and

Ref. #	Listing of Challenged Claims
20.b.4	a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices,
20.c	the method comprising:
20.d.1	receiving a data signal at a first terminal of the plurality of input/output terminals;
20.d.2	receiving control signals at second terminals of the plurality of input/output terminals;
20.d.3	providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and
20.d.4	selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals,
20.e.1	the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die,
20.e.2	the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.
21	The method of claim 20, further comprising: selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver based, at least in part, on a load on the second driver.
22	The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.
23	The method of claim 20, further comprising generating the chip select signals from at least some of the control signals.
24	The method of claim 20, wherein the control signals include the chip-select signals.
25	The method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias.

Ref. #	Listing of Challenged Claims
26	The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die.
27.a	The method of claim 20, further comprising generating data path control signals from at least some of the control signals,
27.b	the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal.
28	The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals.
29.a	A memory module operable via a memory control hub, comprising:
29.b	a register device configured to receive command/address signals from the memory control hub and to generate control signals; and
29.c	a plurality of DRAM packages, each DRAM package comprising:
29.d.1	a plurality of data terminals via which the DRAM package communicates data with the memory control hub, and
29.d.2	a plurality of control terminals to receive the control signals;
29.e	a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;
29.f	at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
29.g.1	a control die comprising
29.g.2	at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and
29.g.3	chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

Ref. #	Listing of Challenged Claims
29.g.4	wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.
30	The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals.
31	The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.
32	The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.
33	The memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals.
34	The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

I. PETITIONER'S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 8,787,060.

The following proceedings are currently pending:

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. amended complaint filed May 3, 2022)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-01427 (U.S. Patent No. 9,318,160)
- U.S. Application No. 17/694,649

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-34 of U.S. Patent 8,787,060 ("060 Patent") (EX1001) based on grounds not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

Petitioner certifies that the 060 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 060 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-34 of the 060 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	1-6, 8-14, 16-19, 29-34	103(a)	Kim+Rajan
2	1-14, 16-19, 29-34	103(a)	Ground 1 + Riho
3	1-6, 8-34	103(a)	Ground 1 + Wyman
4	1-14, 16-19, 29-34	103(a)	Riho+Rajan
5	1-34	103(a)	Ground 4 + Riho2

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above on page vi.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 060 Patent

All the prior art in the Grounds above predates November 3, 2010, when the provisional application for the 060 Patent was filed, but to the extent it matters, the

claims of the 060 Patent do not appear to have support in any application filed before ***November 3, 2011***. EX1003, ¶¶47-50. For example, all the independent claims require "*first*" and "*second*" "*group[s] of … array die[s]*" in a single memory package, but the provisional does not disclose that. EX1005, ¶¶[0006]-[0012], Fig.3 (below); EX1003, ¶¶51-53.

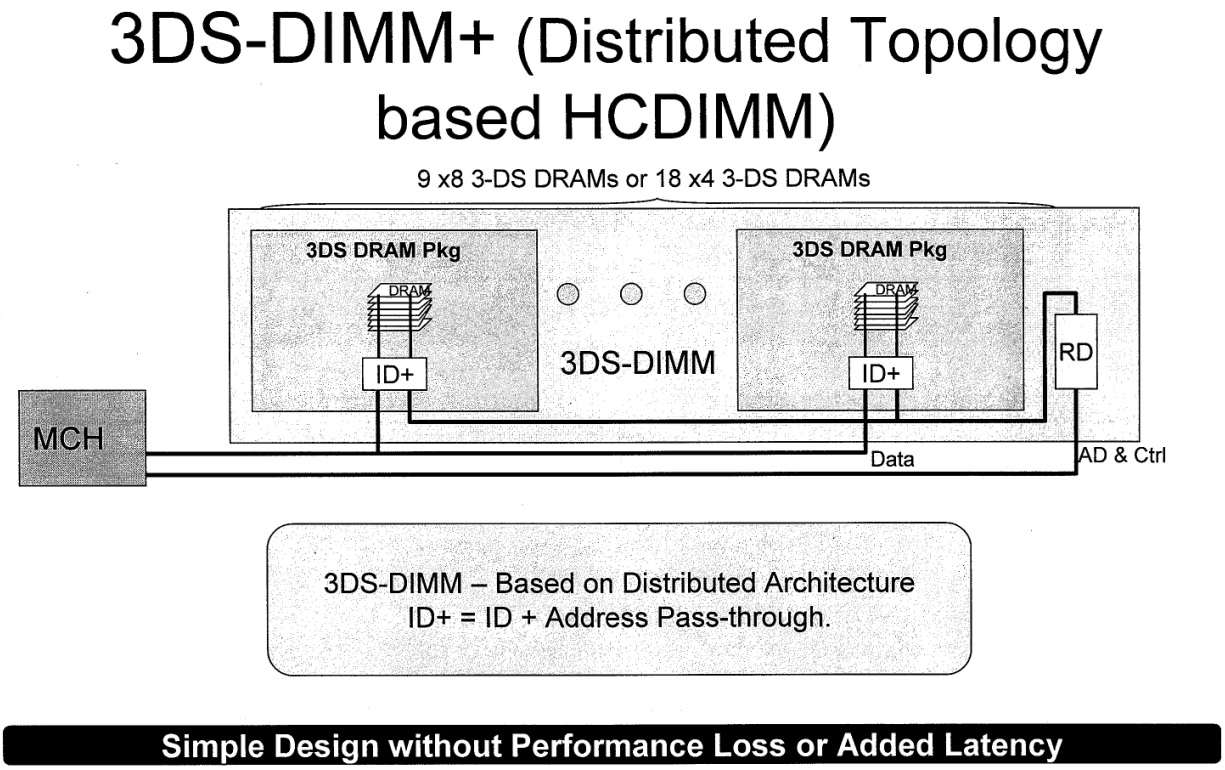


Figure 3

Furthermore, the provisional does not disclose a "*first*" and "*second*" "*die interconnect*" in "*electrical communication*" with one group of array dies but not the other group, as required by all the independent claims, and does not disclose

"*respective states*" of "*data conduits*" as required by independent claims 1, 11, and 29. EX1005, Figs.1-3; EX1003, ¶¶54-59.

B. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 060 Patent in 2010 and 2011 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶60. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads. *Id.*

C. Background Technology

1. JEDEC Standards

As recognized by the provisional application, EX1005, ¶¶[0004-05], a POSITA would have been familiar with the JEDEC standards for memory devices and memory modules. EX1003, ¶¶132-134; EX1023, p.9 & Fig.16; EX1022, pp.332-35, 318-20. For example, a POSITA would have understood that DDR SDRAM memory devices were already standardized by JEDEC. EX1015, 8:6-15; EX1016, ¶[0027]; EX1003, ¶132. Moreover, a POSITA would have understood that JEDEC had standardized memory modules and corresponding interface circuits such as "a register, an AMB, a buffer, or the like." EX1015, 4:20-24; EX1003, ¶132. Examples of relevant standards include the JEDEC standard for DDR3 memory devices, EX1019-21, and the JEDEC specification for GDDR4 memory devices, EX1035.

2. Electrical Load and Drivers

A POSITA would have also been familiar with basic concepts like electrical loads of circuitry used in stacked memory devices and corresponding driving requirements to drive the load of such circuitry. EX1001, 2:8-15 (acknowledging known tradeoff between driver size, load, space, and power); EX1003, ¶135. For example, the greater the "fan-out," the greater the capacitive loading, and thus the greater the propagation delay, as shown below. EX1030, pp.132-138, Fig.3.55 (below); EX1003, ¶136.

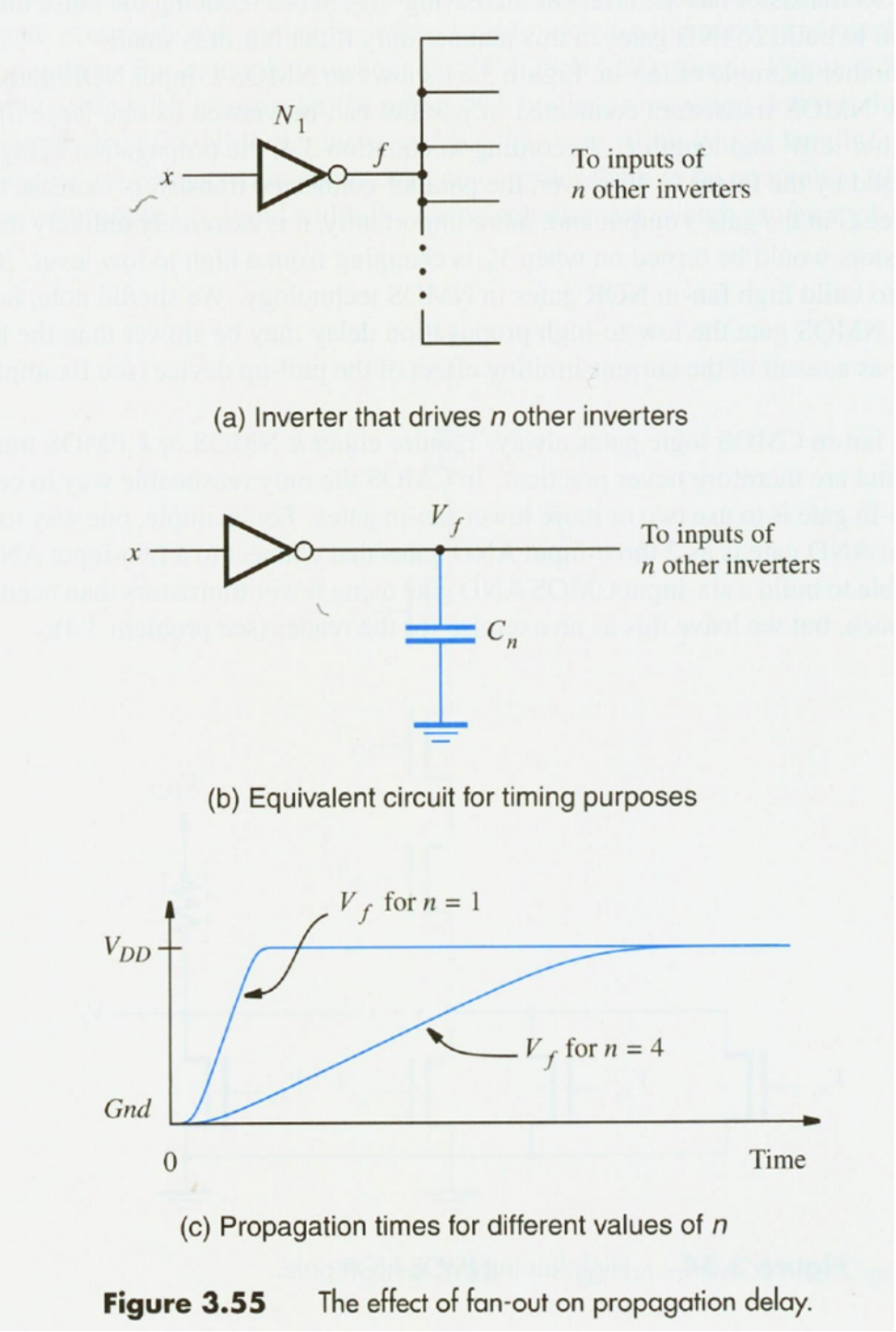


Figure 3.55 The effect of fan-out on propagation delay.

A POSITA would have understood that buffers (such as tri-state buffers) were often used to improve performance when driving a large capacitive load, and

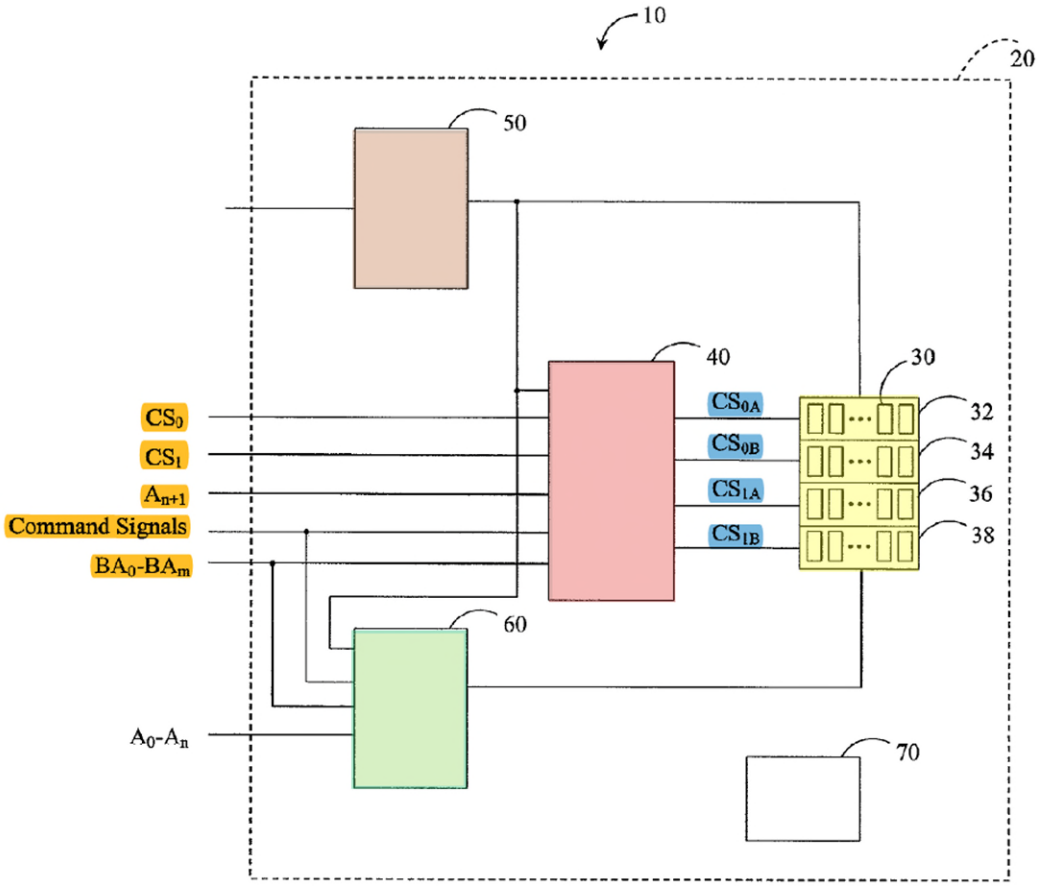
that "[b]uffers can be created with different amounts of *drive capability*." EX1030, pp.135-138; EX1003, ¶137.

3. Rank Multiplication

As admitted by the 060 Patent, a POSITA also would have been familiar with "rank multiplication"—e.g., where a memory module can appear to the computer system as if it has two ranks of higher density (and more expensive) memory devices complying with the JEDEC standard, when it physically has four ranks of lower density (and less expensive) memory devices—which can result in substantial cost savings, providing a motivation to implement the technique in a wide range of memory packages and memory modules. EX1001, 22:37-39 ("Embodiments of rank multiplication are described in greater detail in U.S. Pat. Nos. 7,289,386 ["the 386 Patent," EX1028, 4:47-5:10, 32:58-33:16] and 7,532,537 [EX1031] …."); EX1041, 2:15-19; EX1015, 6:30-7:67; EX1003, ¶138.

As illustrated in Figure 1A (below) of the prior-art 386 Patent, rank multiplication involves mapping chip select signals (e.g., CS_0, CS_1, orange) and address signals (e.g., A_{n+1}, orange) received from a system controller complying with the JEDEC standard into ***more*** chip select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}, blue) to control the higher number of ranks of memory devices (yellow) on the module. EX1028, 2:34-38, 5:11-50, 6:63-8:45, Fig.1A; EX1003, ¶¶139-140.

Figure 1A:



More ranks would result in more load, however, so the prior-art 386 Patent explains that an isolation device (e.g., 120 below) should be used to reduce the electrical load created by the additional ranks of memory devices, and to avoid certain data collisions. EX1028, 24:41-56, 26:12-19, Fig.6D (below); *see also* EX1031, 6:48-62; EX1003, ¶140.

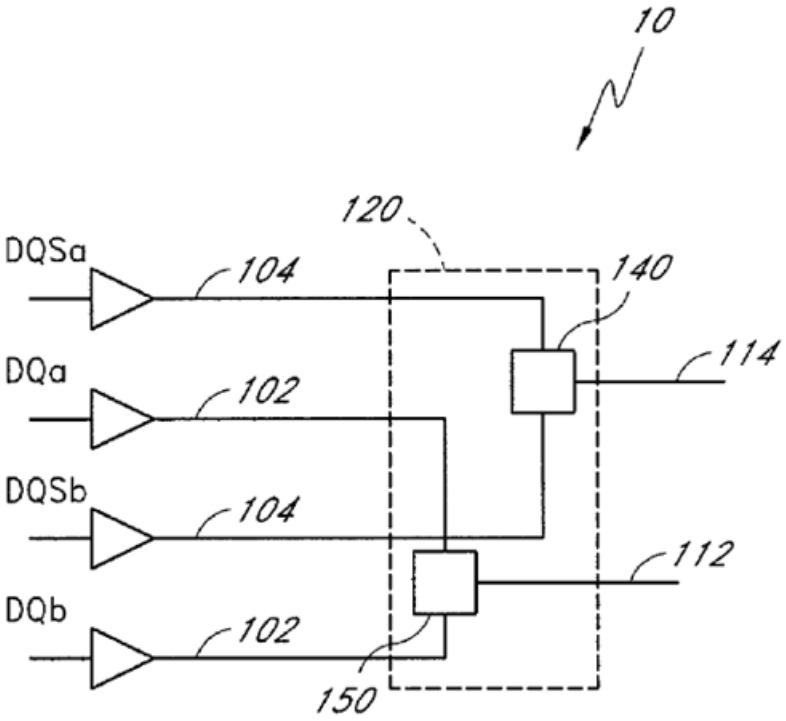


FIG. 6D

While the prior-art 386 Patent discloses rank multiplication implemented in a separate controller (the register), *see* EX1028, 5:42-48, POSITAs would have known that it could ***also*** be implemented within a single memory package on the control die, or in both locations, *see* EX1015, 6:30-7:67; EX1041, 2:15-19; EX1001, 18:38-19:7, Fig.7 (below, showing prior-art module implementing rank multiplication in both the module controller 712 and the memory package control chip 722); EX1003, ¶141.

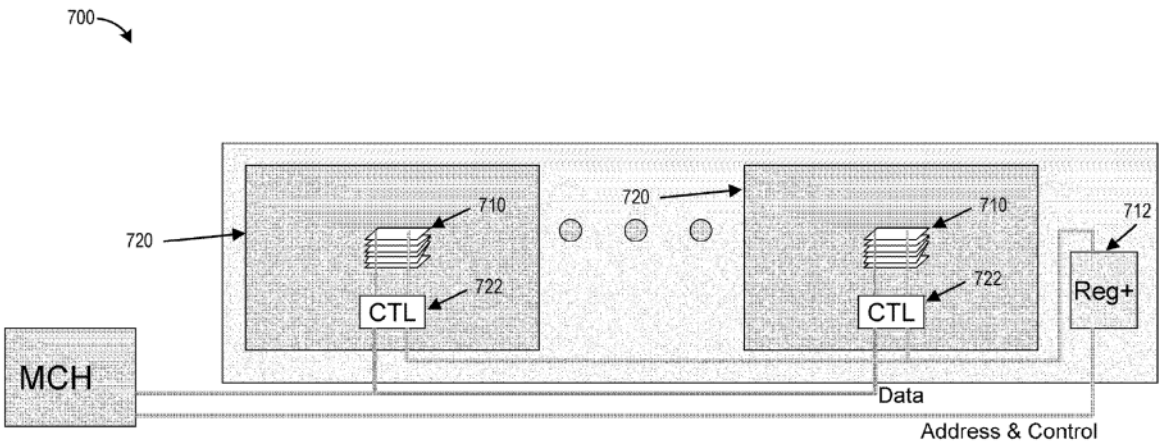


FIG. 7

D. The 060 Patent

1. Technical Overview

The 060 Patent "relates to memory devices and memory modules …. specifically … [ways] for reducing the load of drivers of memory packages included on the memory modules." EX1001, 1:18-22.

The 060 Patent admits as prior art the memory package designs depicted in Figures 1A and 1B (annotated below),[1] which include, for example, "array dies 160 [(yellow)] and a control die 170 [(green)] that…[includes] a driver 184 that drives data signals to each of the array dies 160 along a corresponding die

[1] Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.

interconnect 182 [(light green)]." EX1001, 1:30-33, 1:63-2:4, Fig.1B; EX1003, ¶61.

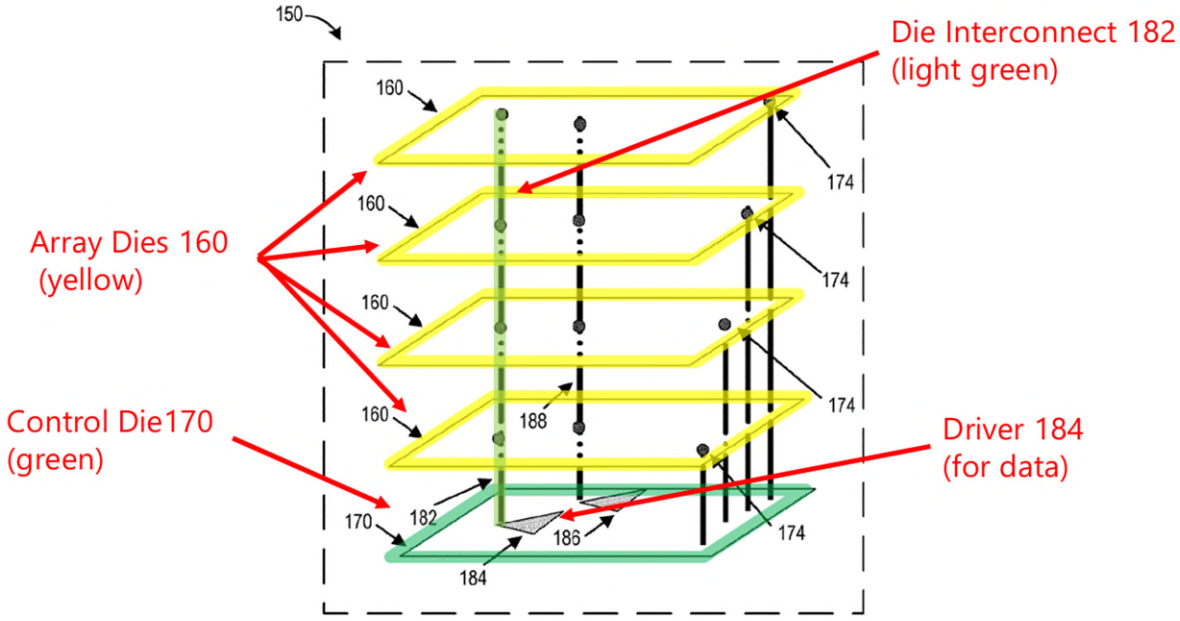
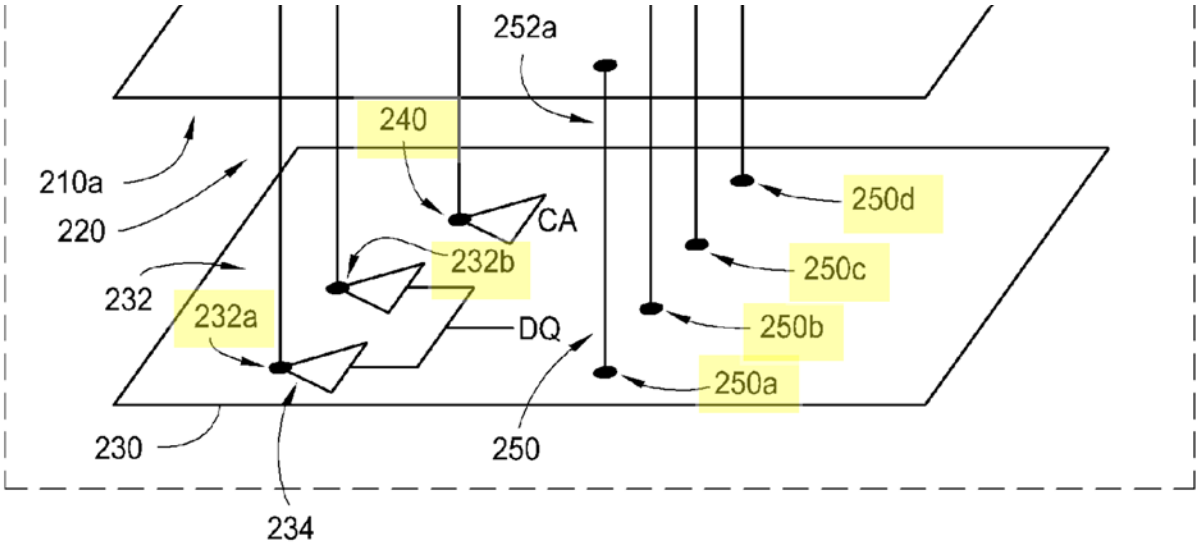


FIG. 1B

The 060 Patent teaches that each die interconnect has a corresponding "conduit" (e.g., 232a below), configured to transmit a signal to the die interconnect, and which may include a driver. EX1001, Fig.2, 6:48-62, 9:28-60, 21:18-20; EX1003, ¶62.



As illustrated by Figure 2 (below), the 060 Patent purports to improve upon the prior art (e.g., Figure 1B) by replacing ***one*** data driver (e.g., driver 184 in Figure 1B) with ***two*** or more drivers 234 coupled to the same DQ data terminal, each driving the data signal through a respective die interconnect (220a, 220b) in electrical communication with a ***subset*** of the array dies, thereby reducing the overall load of each data conduit. EX1001, 1:19-21, 1:63-2:4, 2:8-15, 7:9-8:18, Fig.2; EX1003, ¶¶61-63.

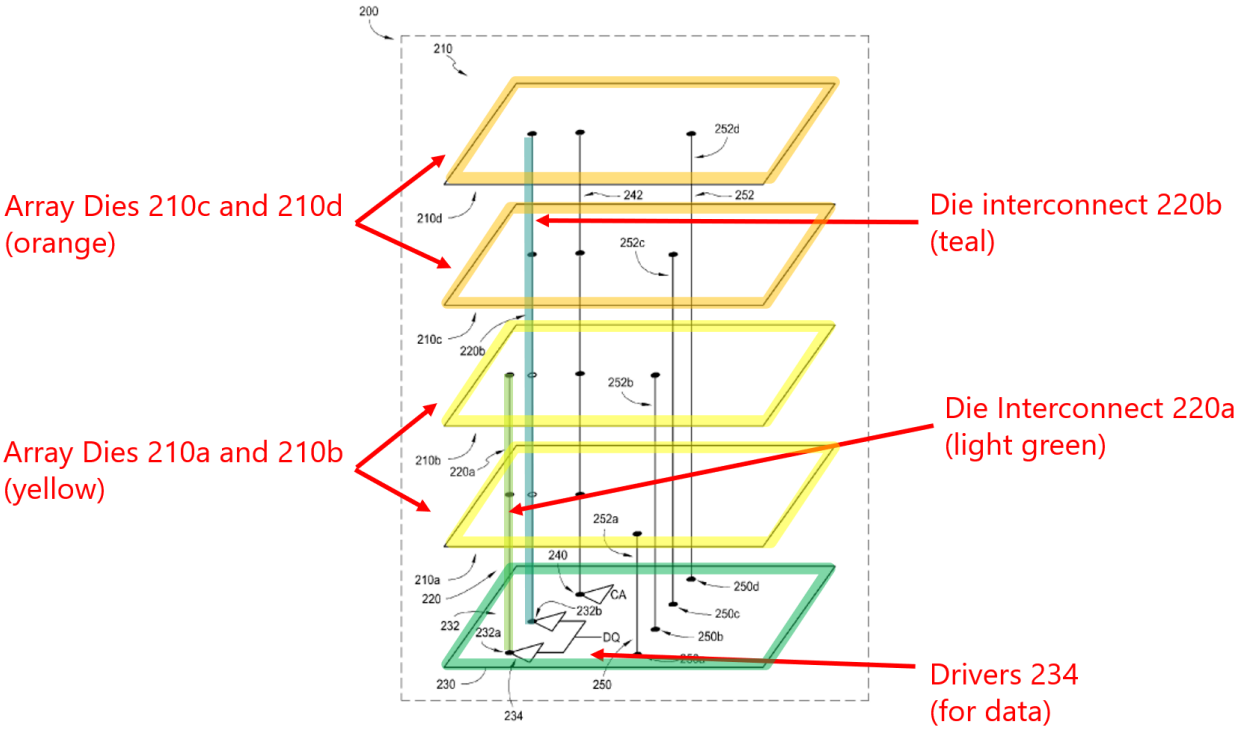


FIG. 2

In Figure 2, for a given data bit (e.g., D0), die interconnect 220a (light green) may be in electrical communication with data ports from array dies 210a and 210b (yellow) (illustrated by darkened circles) and not in electrical communication with data ports from array dies 210c or 210d (orange), while die interconnect 220b (teal) may be in electrical communication with data ports from array dies 210c and 210d and not 210a and 210b, even though die interconnect 220b may pass through these array dies (illustrated by unfilled circles), "e.g., through through-holes or vias of array dies 210a and 210b." EX1001, 5:63-6:1, 6:9-15; EX1003, ¶¶64-65.

2. Prosecution History

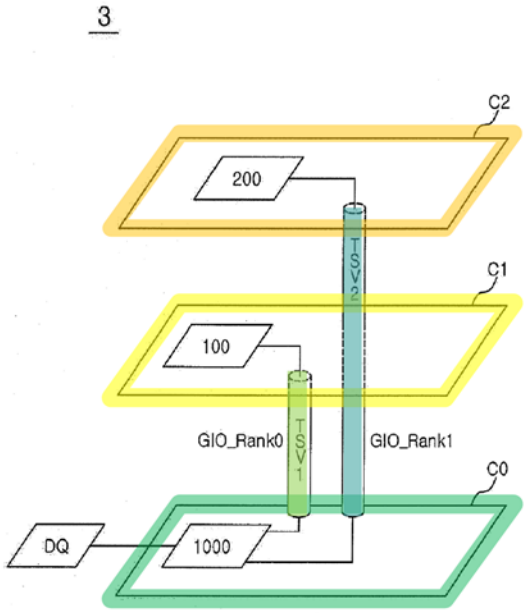
During prosecution, the independent claims (and others) were rejected as anticipated by Rajan137 (EX1011) (different than the Rajan reference relied upon in this Petition). EX1002, pp.238-48, 433-443; EX1003, ¶¶68-72. In response, Patent Owner argued that Rajan137 "merely stacks DRAM circuits 206A-D, which are different from array dies," and "[a]s a result, Rajan[137]'s buffer chip 202 operates very differently" from the claimed control die. EX1002, pp.465-66; EX1003, ¶73. The Examiner allowed the claims, with minor Examiner's amendments, but without any stated reasons for allowance. EX1002, pp.474, 478-80; EX1003, ¶¶74-75. A series of later-filed applications claiming priority to the 060 Patent were allowed after the filing of terminal disclaimers, but without any further discussion of prior art. EX1006-EX1010; EX1003, ¶¶76-106.

V. OVERVIEW OF THE PRIOR ART

A. Kim (EX1014)

U.S. Patent Publication No. 2011/0103156 ("Kim"), filed in 2009 and published May 5, 2011, is prior art at least under §102(e). EX1014, 1. Kim discloses one or more main chips, e.g., C0 (green) and two or more slave chips, e.g., C1 (yellow) and C2 (orange), the chips being connected by through-silicon vias (TSVs) (light green and teal, respectively). EX1014, ¶¶[0047-48], Fig.5 (below); EX1003, ¶¶115-118.

FIG.5



B. Rajan (EX1015)

U.S. Patent No. 8,041,881 ("Rajan"), filed in 2007 and issued October 18, 2011, is prior art at least under §102(e). EX1015, 1. Rajan discloses making high-capacity memory using low-cost memory chips, e.g., using stacked DRAM memory chips (yellow, orange) and a buffer chip (green) for interfacing with a host system, and connecting the stacked DRAM chips and the buffer, e.g., using two data busses (light green and teal). EX1015, 1:51-60, 4:48-50, Fig.4 (below); EX1003, ¶¶119-120.

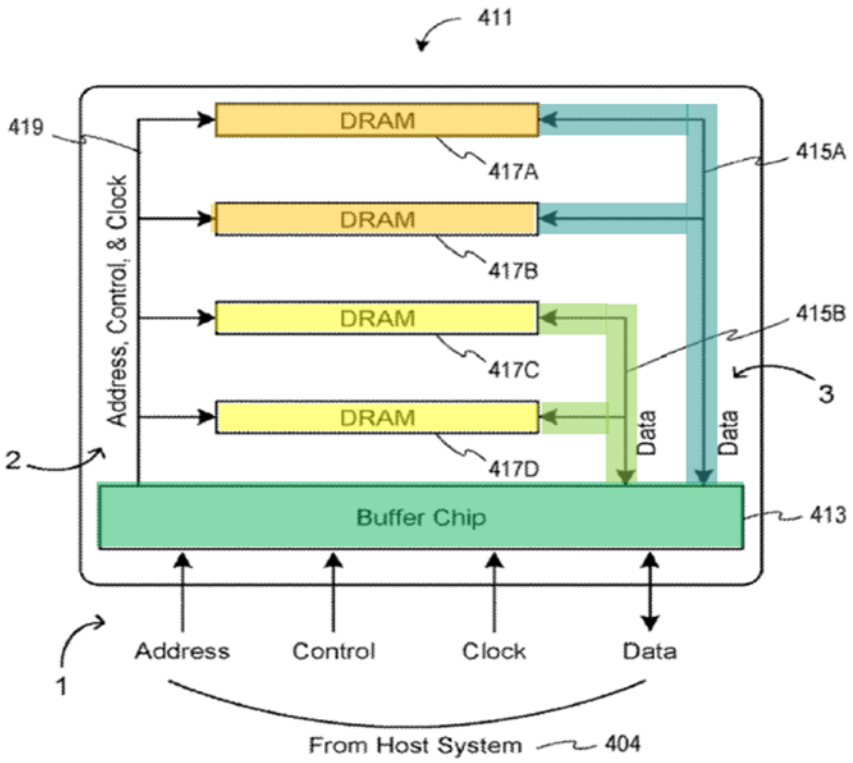


FIG. 4

Rajan further discloses its interface with the host can comply with JEDEC standards. EX1015, 4:20-24, 14:11-18, Fig.18 (below); EX1003, ¶121.

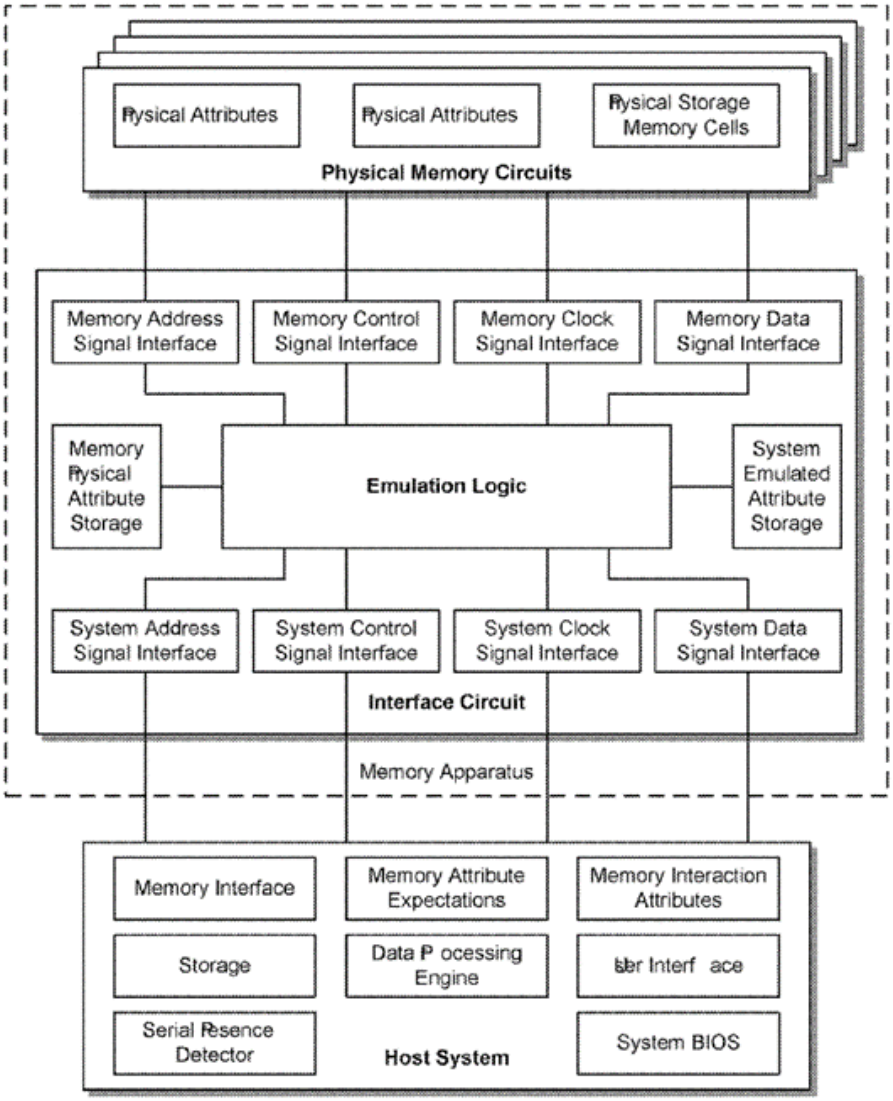


FIG. 18

C. Riho (EX1016)

U.S. Patent Publication No. 2011/0026293 ("Riho"), filed July 16, 2010, and published February 3, 2011, is prior art at least under §102(e). EX1016, 1. Riho discloses a memory package with a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15), organized into pairs, connected to the control chip by through-silicon vias (TSVs), "to reduce by half the load … as compared

with the case where the SDRAM chips are not divided into groups." EX1016, ¶[0103], Figs.1-2 (below); EX1003, ¶¶122-125.

FIG. 1

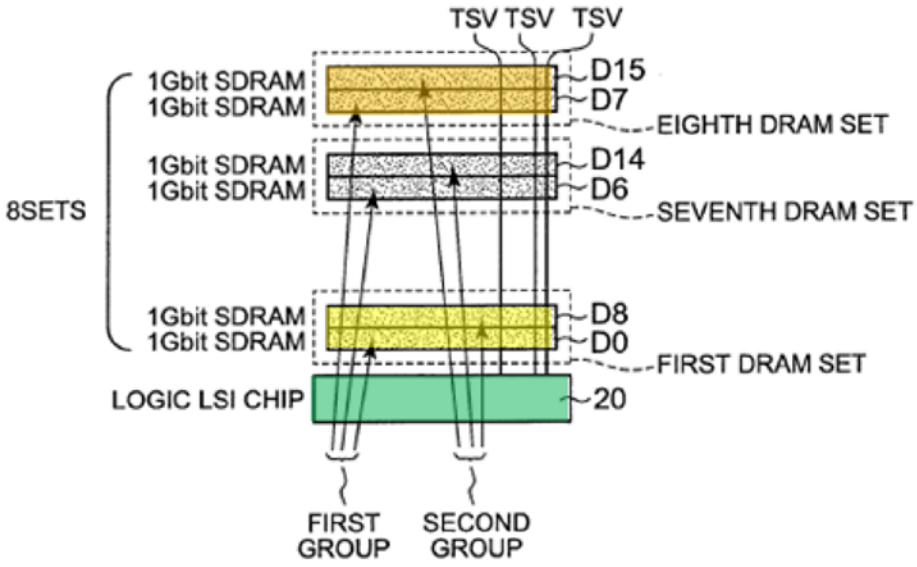
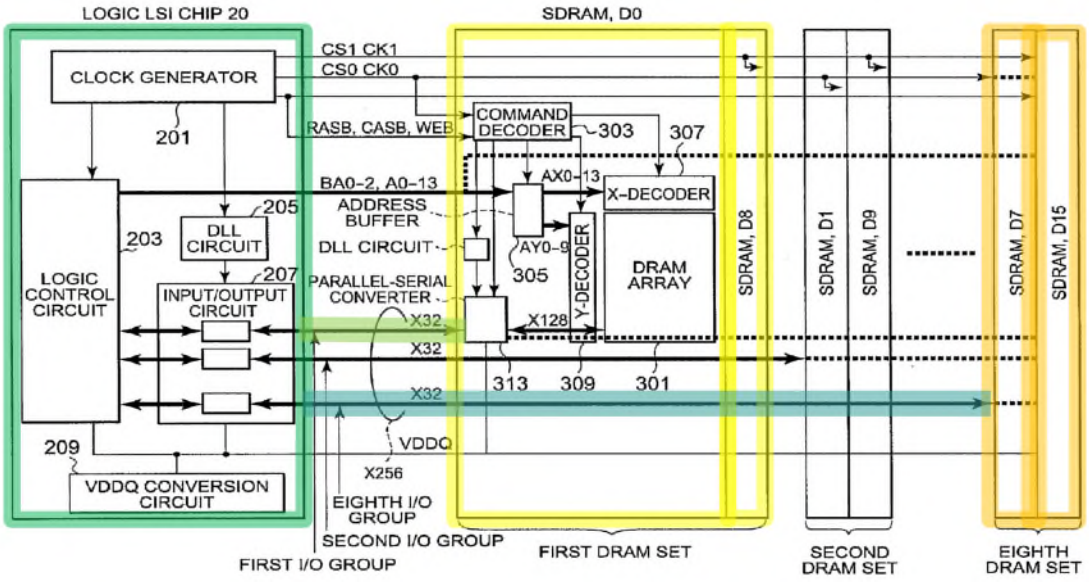


FIG. 2



D. Wyman (EX1017)

U.S. Patent No. 7,969,192 ("Wyman"), filed March 26, 2010, and issued June 28, 2011, is prior art at least under §102(e). EX1017, 1. Wyman discloses that when chips are stacked, shorter paths (e.g., 802) require less drive, while longer paths (e.g., 804) require a larger drive due to "increased resistance, capacitance and impedance," but it would be "wasteful" and "overkill" to use the "full capacity" of a driver for either path. EX1017, 1:22-24, 1:45-48, 6:15-50, Fig.8 (below); EX1003, ¶¶126-128.

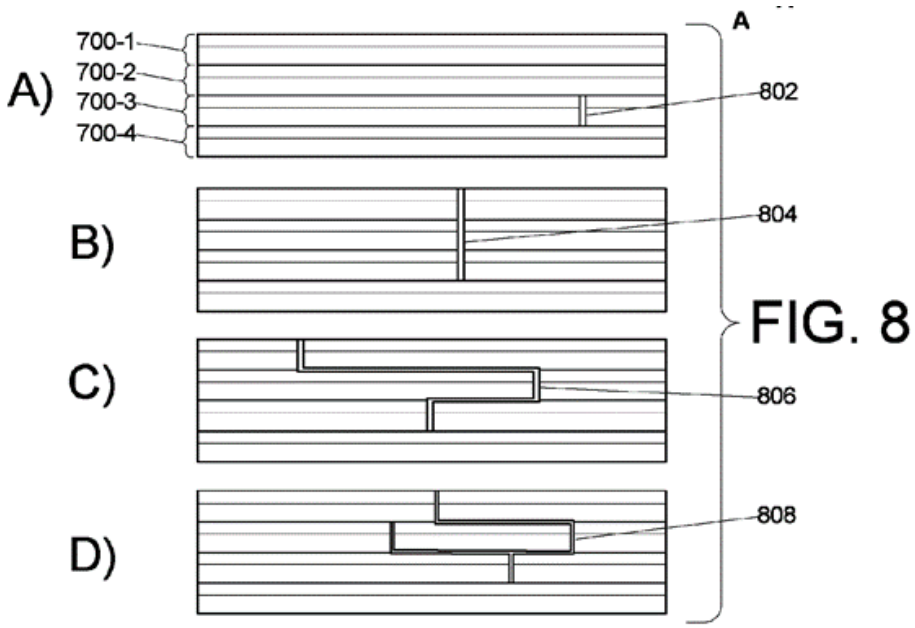


FIG. 8

E. Riho2 (EX1018)

U.S. Patent Publication No. 2010/0195364 ("Riho2"), published August 5, 2010, is prior art at least under §102(a). EX1018. Riho2 has the same inventor as Riho above, EX1016. Riho2 recognizes that the capacitive load will increase "as the number of stacked chips is increased," and thus discloses a circuit for

optimizing output drive capacity "according to a change in the time constant caused by parasitic capacitance and parasitic resistance." EX1018, ¶¶[0003, 0010, 0097], Fig.7A (below); EX1003, ¶¶129-131.

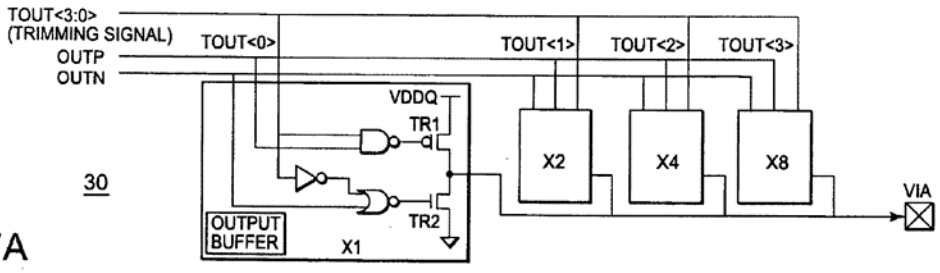


FIG. 7A

VI. CLAIM CONSTRUCTION

In related litigation, Patent Owner has interpreted some claim terms broadly for purposes of infringement, *see* EX1044, pp.63-68; EX1046, pp.63-69, even though a narrower interpretation may be more reasonable, but Petitioner contends that no express constructions are needed for this proceeding because the claims are obvious under either interpretation. EX1003, ¶112-113.

VII. ARGUMENT

A. Ground 1 (claims 1-6, 8-14, 16-19, 29-34)

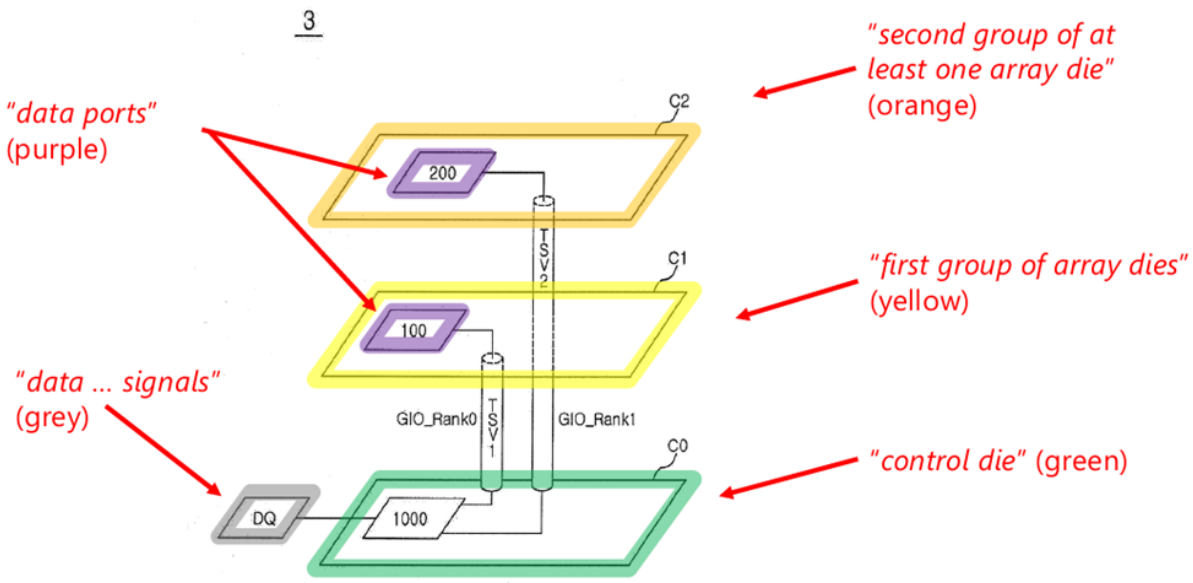
1. Ground 1 combination: Kim (EX1014) and Rajan (EX1015)

Ground 1 combines Kim (EX1014) with Rajan (EX1015), both of which, like the 060 Patent, disclose the same basic memory package structure including groups of stacked memory chips (yellow, orange) and a shared interface circuit (green). EX1014, ¶¶[0012, 50], Fig.5 (first below); EX1015, 1:51-60, 2:6-7, 4:48-

50, Fig.4 (second below); EX1001, 1:18-21, 5:23-26, Fig.2 (above p.14); EX1003, ¶¶150, 154-155.

Kim:

FIG.5



Rajan:

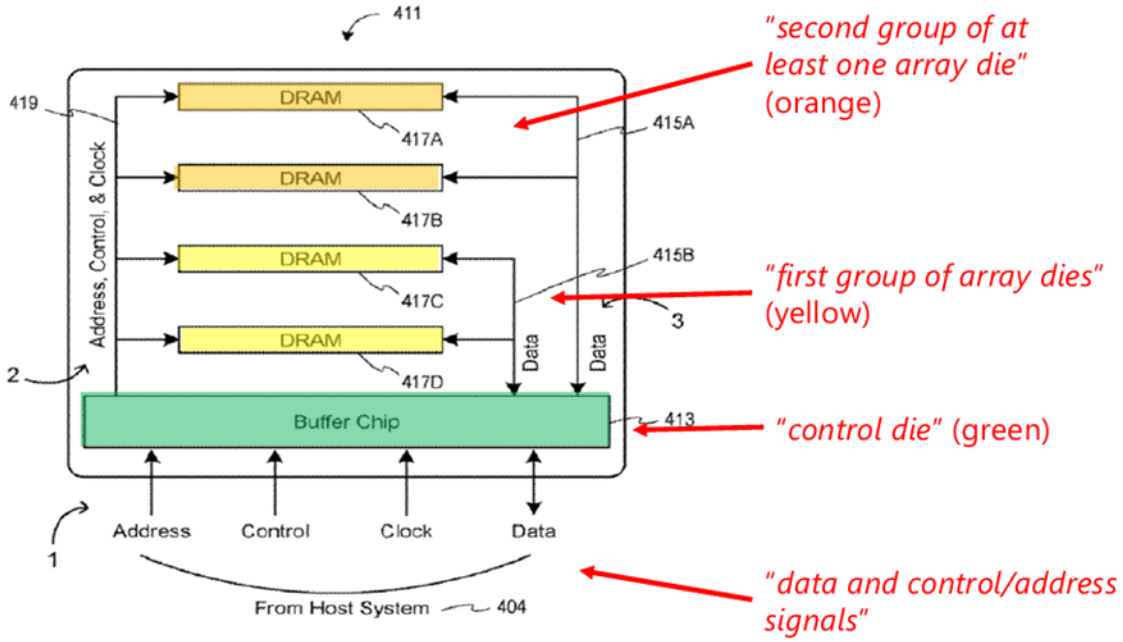


FIG. 4

A POSITA would have been motivated to combine Kim and Rajan for several reasons. First, as explained and shown above, they are analogous art with similar structures, so a POSITA would be motivated to look at the details taught by Rajan when implementing Kim, including details about the interface chip (green) and stacking the dies (yellow, orange). EX1003, ¶¶154-155.

Second, a POSITA would be motivated to create a package with an interface that complied with the well-known JEDEC standards, as taught by Rajan. EX1003, ¶¶152-153. Specifically, a POSITA would have found it obvious to use Rajan's terminals (e.g., in Figure 4, above) and corresponding data and control/address signals, in Kim's stacked memory package (e.g., in Figure 5, above), and been motivated to implement the functionality of a JEDEC compatible external data interface in Kim's control chip, as suggested by Rajan (including Figure 18, below), to make Kim's memory package compatible with the JEDEC standard. EX1014, ¶[0038], Fig.5; EX1015, 3:52-54, 8:8-11, Figs. 4, 18 (below); EX1003, ¶¶151-153. Indeed, the JEDEC standards were influential and well-known, as discussed above (p.6).

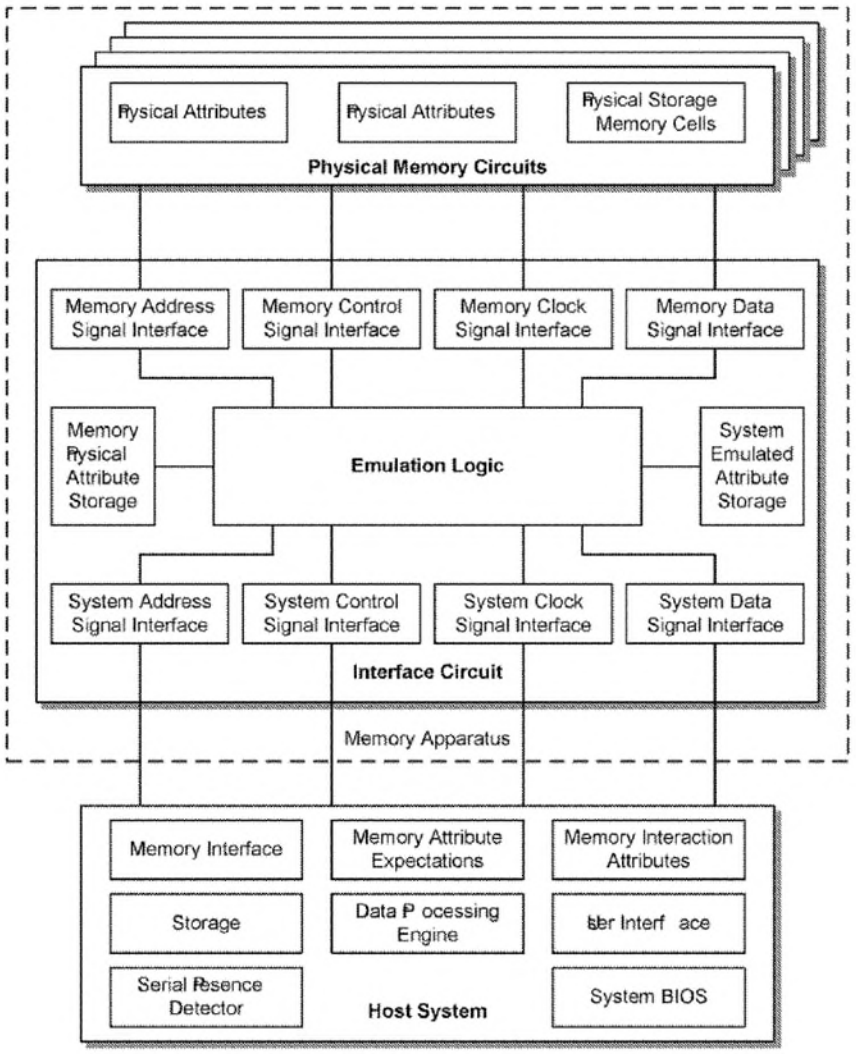


FIG. 18

Such a combination — following Rajan's suggestion to implement address, control, and data terminals following the JEDEC standards (including the DDR3 standard for stacked memory devices shown below, EX1019, p.12, Fig.3) — would have been well within a POSITA's level of skill since, as demonstrated by the 060 Patent's admitted prior art, emulating a standard JEDEC interface was a known option (as discussed above, pp.8-11). EX1003, ¶¶155-157; EX1001, 22:37-39; EX1015, 5:36-43, 4:20-24, Fig.4.

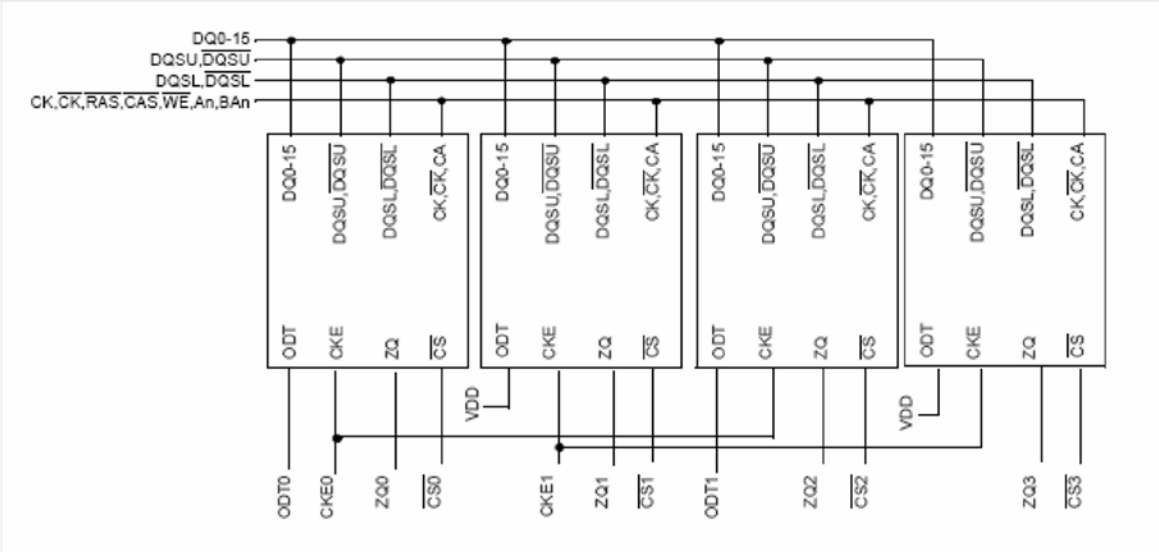
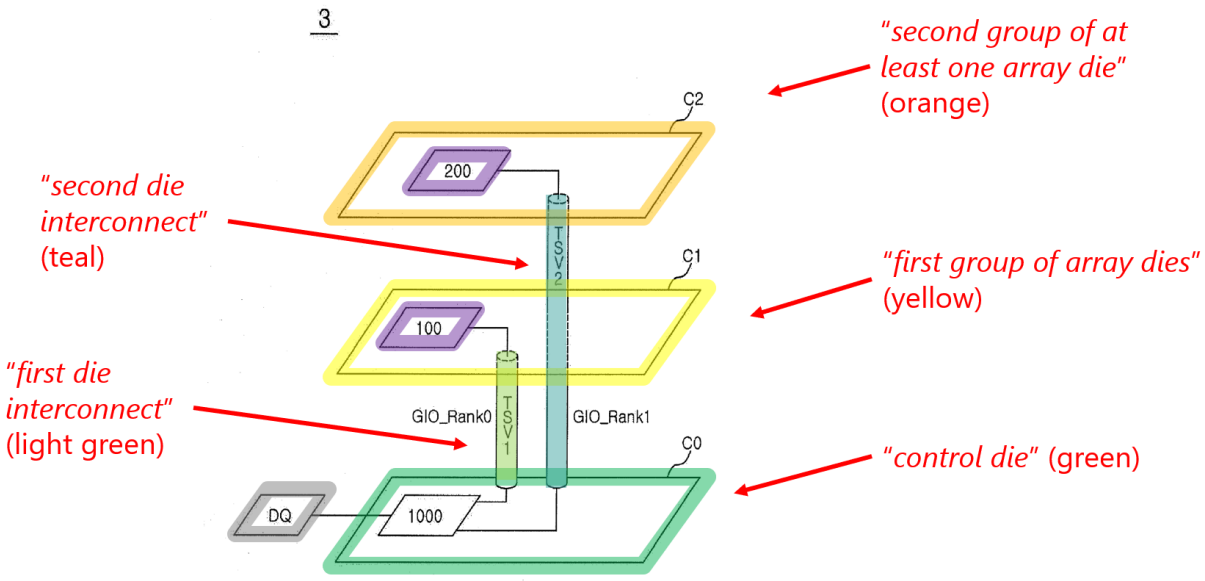


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

Third, a POSITA would have been motivated to look at Rajan for the details about adding more memory chips in the stack (resulting, e.g., in four chips, yellow and orange, in two groups, as shown below), as suggested by Kim's disclosure that "any number of … chips may be used." EX1003, ¶¶158-160; EX1014, ¶¶[0048, 50].

Kim:

FIG.5



Rajan:

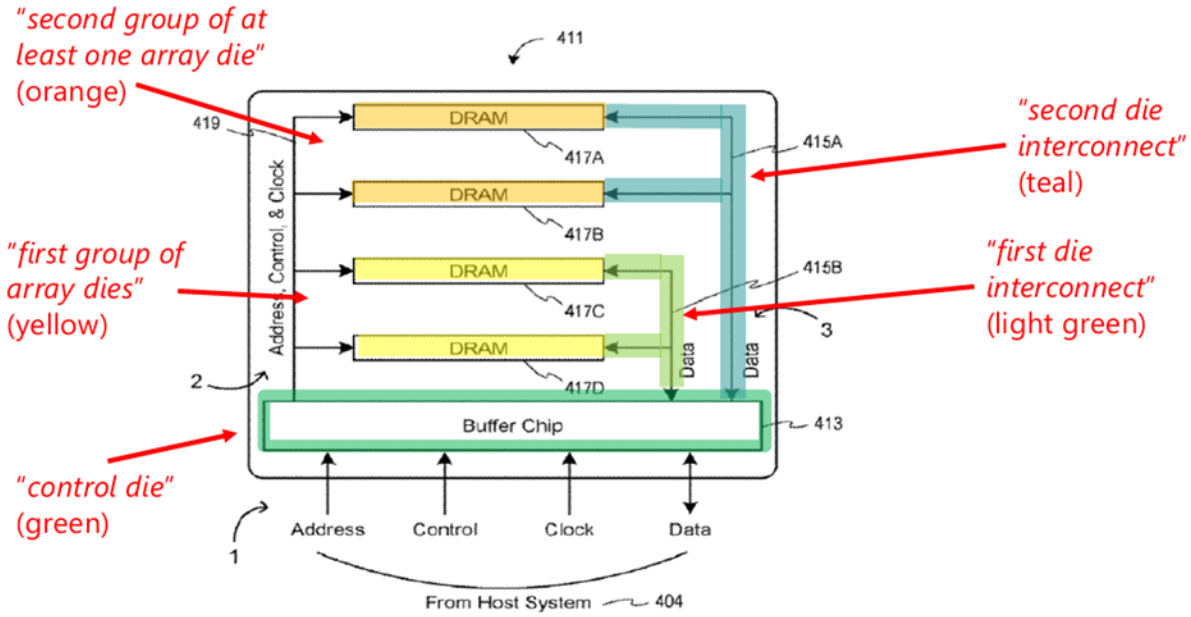


FIG. 4

A POSITA would have been motivated to implement a shared data bus for multiple memory chips as taught by Rajan (e.g., 415A and 415B, above) using, e.g., Kim's TSV interconnects (light green and teal, above), in part because a POSITA would have understood that there were a finite number of known ways to connect additional dies, including having a subset of dies sharing a through-silicon via (TSV). EX1003, ¶¶161-163; EX1015, 5:36-43, Figs. 2-6. Sharing a TSV among two or more dies was a known option, as confirmed by other references at the time (below). *See, e.g.*, EX1025, Fig.5 (below).

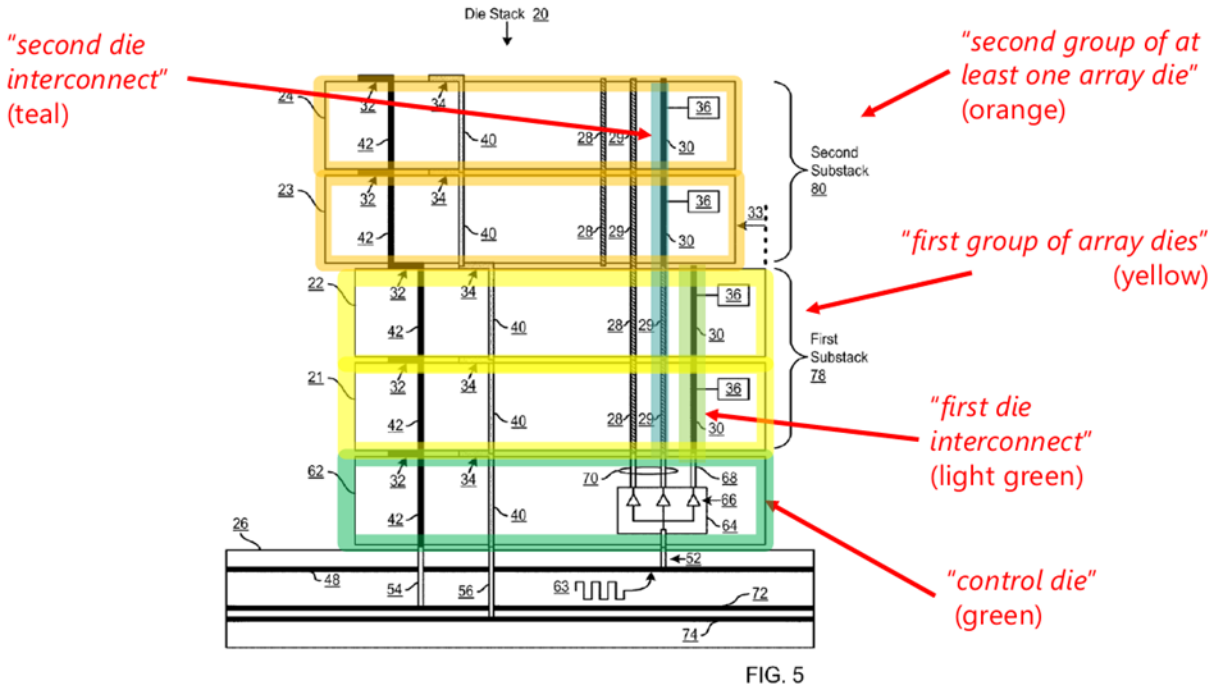


FIG. 5

Moreover, a POSITA would have been motivated to connect additional memory dies to Kim's TSV1 and TSV2 because it would not require creating new TSVs (which would add space and circuitry) and would allow emulating the JEDEC

standard required by external devices. EX1003, ¶164; EX1015, 3:27-30, 3:52-61. Furthermore, it was common at the time to have multiple memory dies sharing a single data bus. EX1003, ¶¶165-166. For example, when implementing "rank multiplication" (discussed above, pp.8-11), it was common to use a "fork-in-the-road" arrangement with two data buses for two ranks of memory devices (shown below left, yellow and orange), with the option of adding two additional ranks of memory devices (resulting in four ranks) to the existing data busses (shown below right, two yellow, two orange), meaning two memory dies (e.g., two orange) would share a given data bus. EX1003, ¶165; EX1026, Figs.12-13 (below); EX1027, pp. 77-82 (Final Written Decision analyzing EX1026); *see also supra* pp.8-11; EX1001, 18:65-19:7, 19:41-47, 22:34-57.

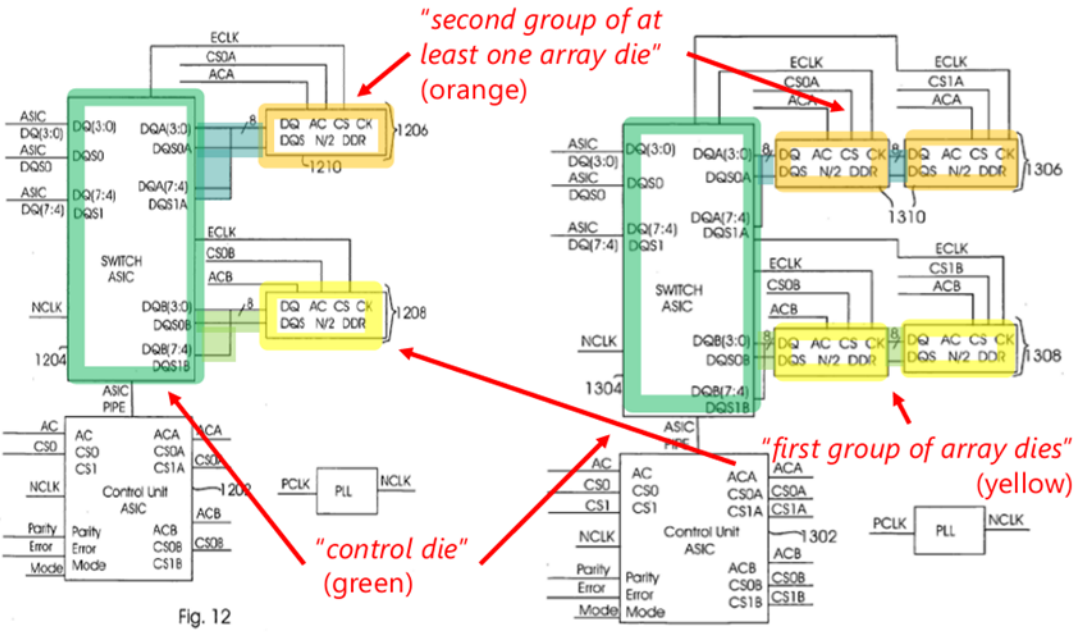


Fig. 12

Fig. 13

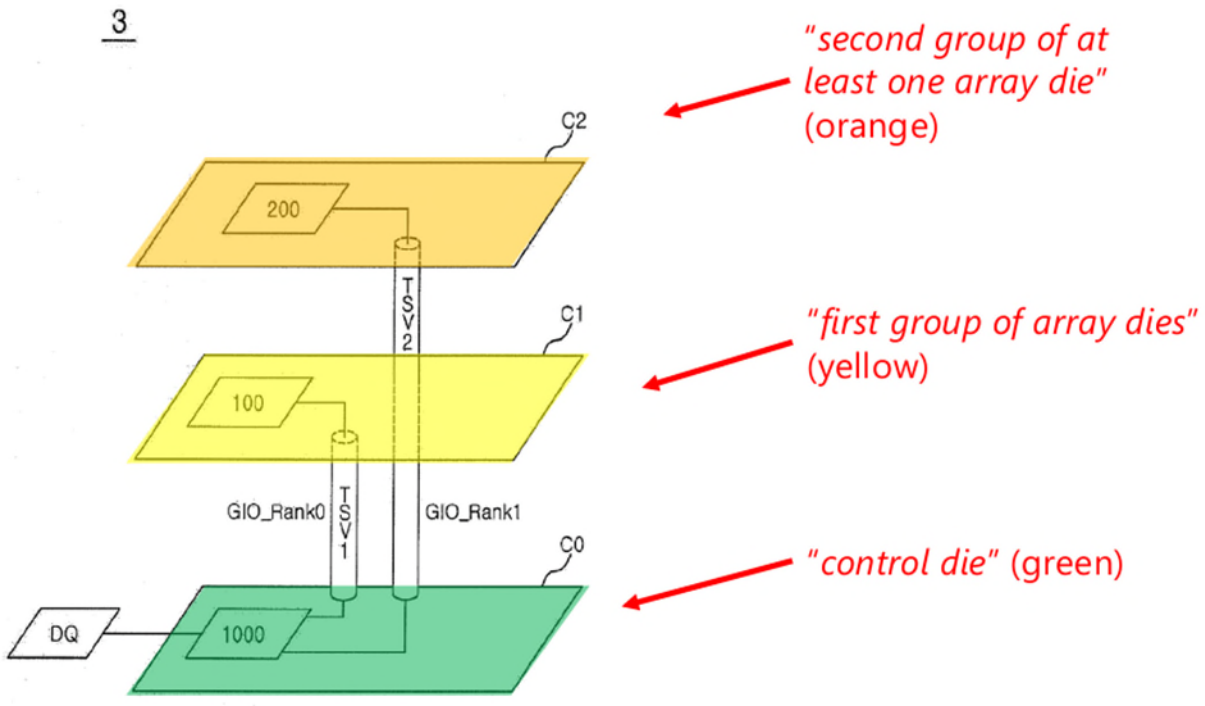
Figure 4 of Rajan teaches a similar arrangement as shown above (p.27), and a POSITA would have been motivated to implement that arrangement in Kim to preserve Kim's data collision avoidance feature without creating additional TSVs. EX1003, ¶167; EX1014, ¶¶[0042-44], Figs.4A-4B.

2. Independent Claim 1

a) ***[1.a] Preamble***

To the extent the preamble is limiting, Ground 1 teaches "*[a] memory package* [e.g., Kim's main chip C0 and stacked memory chips C1 and C2 in Figure 5 (below) which are "package[d] in a single package," EX1014, ¶¶[0046-47]], *comprising*." EX1003, ¶¶184-188.

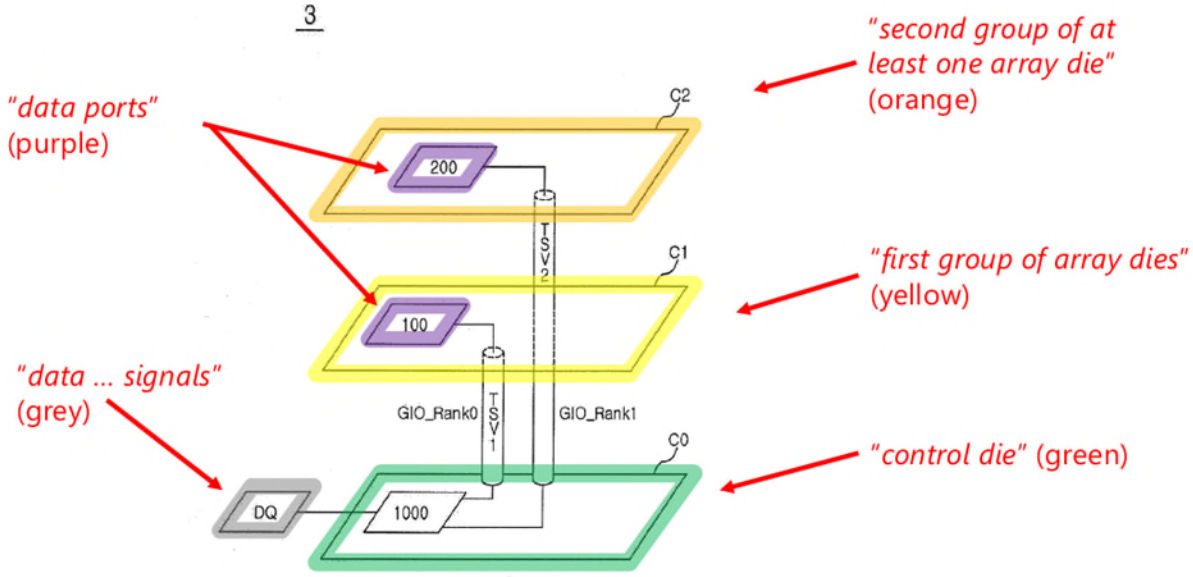
FIG.5

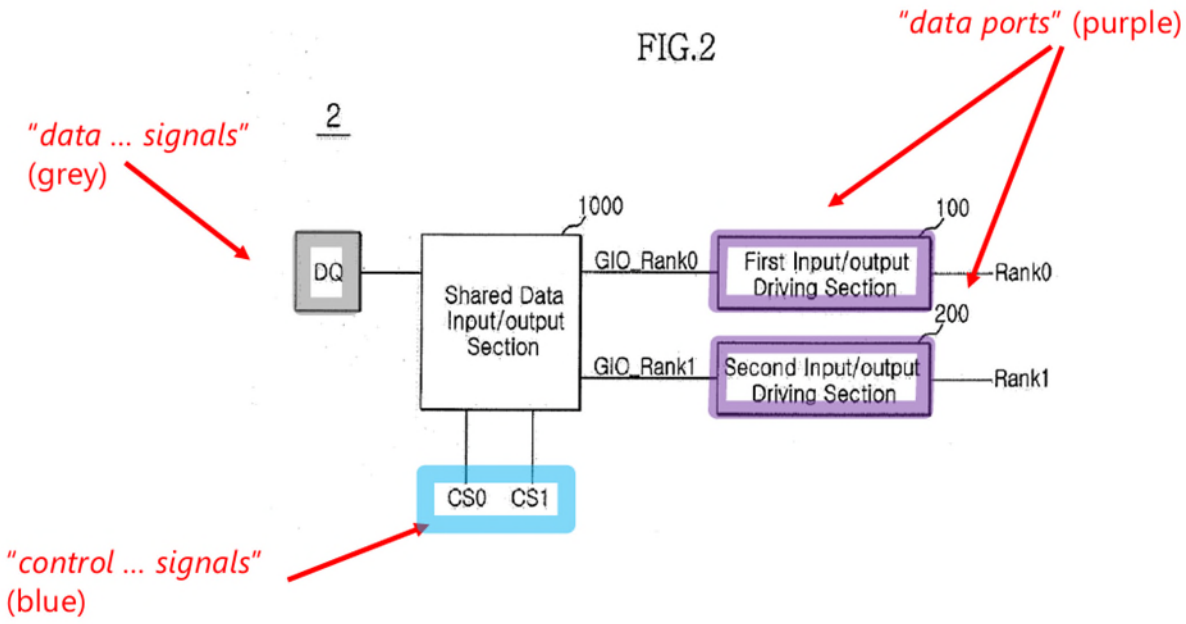


b) ***[1.b] Input/Output Terminals***

Ground 1 teaches "*a plurality of input/output terminals via which the memory package communicates data* [e.g., through Kim's data pad DQ (grey) in Figure 5 (below)] *and control/address signals* [e.g., read/write command signals including chip-select control signals CS0 and CS1 in Figure 2 (below) and address signals A0-A15 per the JEDEC standard, e.g., EX1019, pp.6-13, 18, 33] *with one or more external devices*." EX1003, ¶¶189-210.

FIG.5





Kim describes the input/output section 1000 communicating "*data…signals*" through a data pad "DQ" (grey above) during read and write operations. EX1014, Abstract, ¶[0028]; EX1003, ¶¶193-195.

In Ground 1 (pp.21-30), it would be obvious for Kim's signals to comply with JEDEC. Thus, Kim's chip selection signals CS0 and CS1 would be "*control…signals*" that are part of the command signals that control the memory devices. EX1014, ¶¶[0006, 0032], Fig.2 (above); EX1019, p.13 (chip select signals are "considered part of the command code"). Under the JEDEC standards for stacked memory devices, and as admitted by the 060 Patent, chip-select signals are received from an "*external device[]*" at terminals on the memory package. *See, e.g.*, EX1019, pp.6-14 (describing pinout for stacked memories including terminals for data (DQ) and chip-select (CS) signals); EX1001, 1:30-56 (admitting prior art

included memory packages with chip-select ports "configured to receive corresponding chip select signals to enable or select the array dies for data transfer."); EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35; EX1003, ¶196.

Under the JEDEC standards, Kim's "write and read command signals," EX1014, ¶[0038], would also include "*address signals*" received via terminals from an external controller ("*external device[]*"). *See, e.g.*, EX1019, pp.6-14 (package pinout for stacked DDR3 memories including terminals for address signals A0-A15), p.18 (explaining that read/write commands use row and column address signals), p.33 (Command Truth Table with Activate command with row address, and Read/Write command with column address); EX1001, 1:30-56 (admitting prior art included "command and/or address signals"); EX1003, ¶¶197-198.

Furthermore, a POSITA would have been motivated to implement Kim's control/address signals in light of Rajan (*see* pp.21-30), including Rajan's interfaces for sending/receiving address, control, and data signals to/from the host system in accordance with the JEDEC standards discussed above. EX1015, 2:6-7, 4:20-24, 5:36-43, 14:11-18, Figs.4 (below), 18 (interface circuit); EX1003, ¶¶201-202.

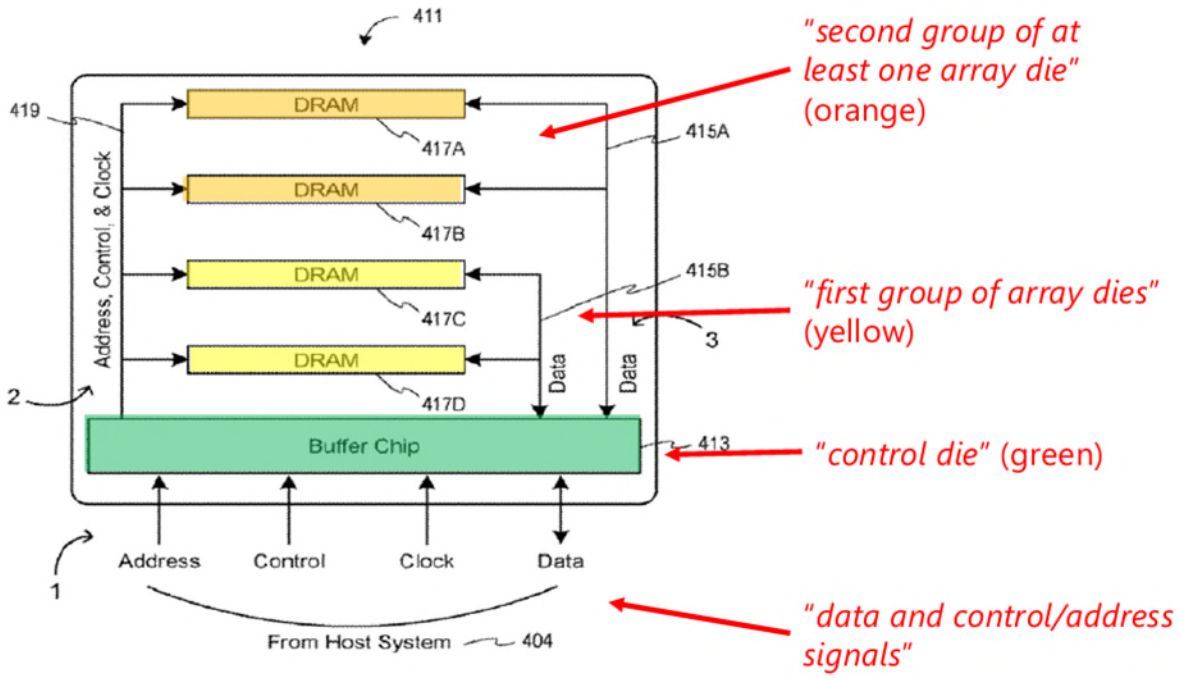
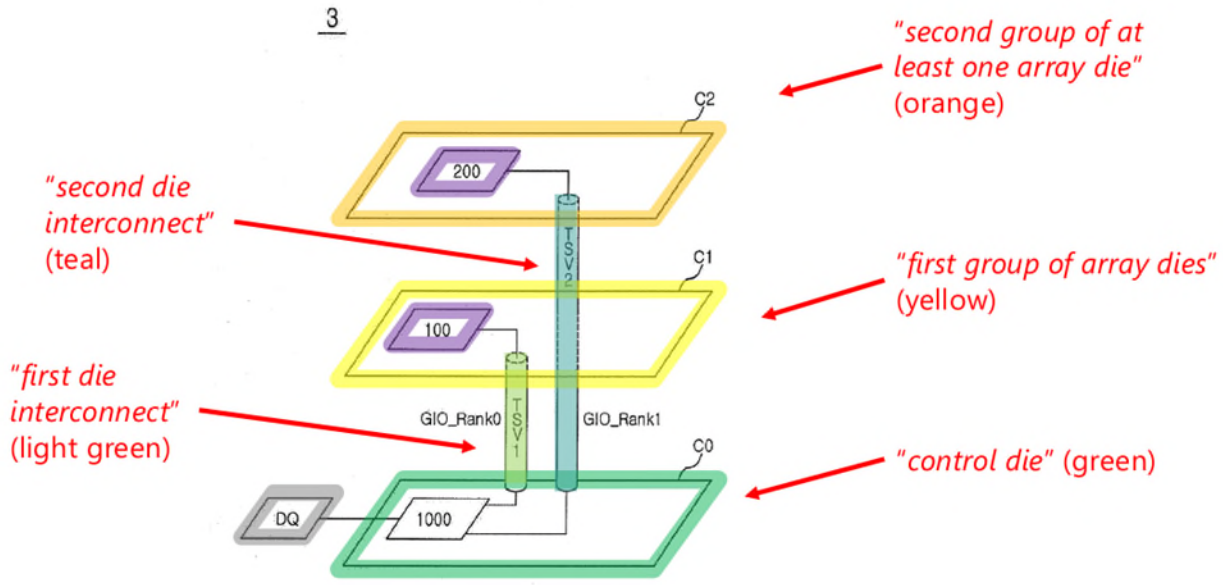


FIG. 4

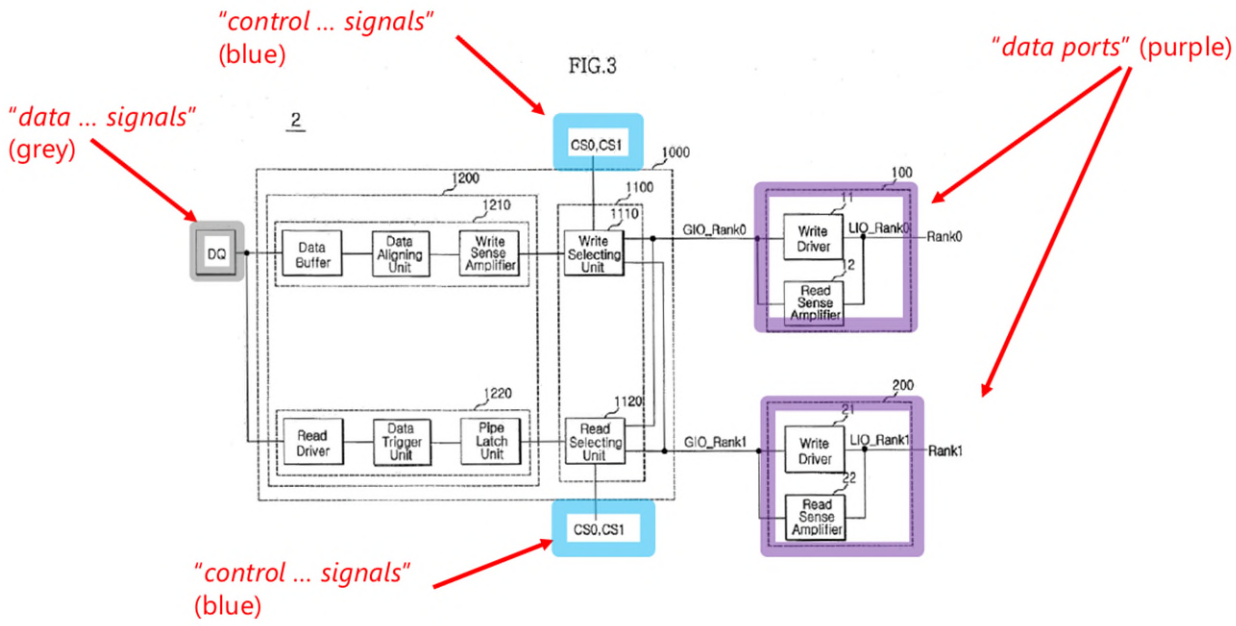
c) ***[1.c] Stacked Array Dies***

Ground 1 teaches "*a plurality of stacked array dies including a first group of array dies* [e.g., including Kim's slave chip C1 (yellow), coupled to TSV1] *and a second group of at least one array die* [e.g., including Kim's slave chip C2 (orange), coupled to TSV2], *each array die having data ports* [e.g., input/output driving sections 100 and 200 (purple)]." EX1014, ¶[0048] ("any number of … slave chips may be used"), Fig.5 (below); EX1003, ¶¶211-229.

FIG.5



A POSITA would have understood from Kim's explanation how the first and second input/output driving sections 100 and 200 store and drive data that they are "*data ports*" through which data is transmitted for storage and through which the stored data is retrieved from the slave chip. EX1014, ¶[0026], Figs.5, 3 (below); EX1003, ¶¶215-216.



A POSITA would further have understood that Kim's "memory bank" for data storage in slave chips C1 and C2 would include a memory array (consistent with textbooks, below, and the JEDEC standards), rendering obvious the claimed "*array die[s]*." *Id.*; EX1019, p.13; EX1023, pp.1-2, Fig.2 (below); EX1022, pp.316-320 (same); EX1003, ¶¶217-218.

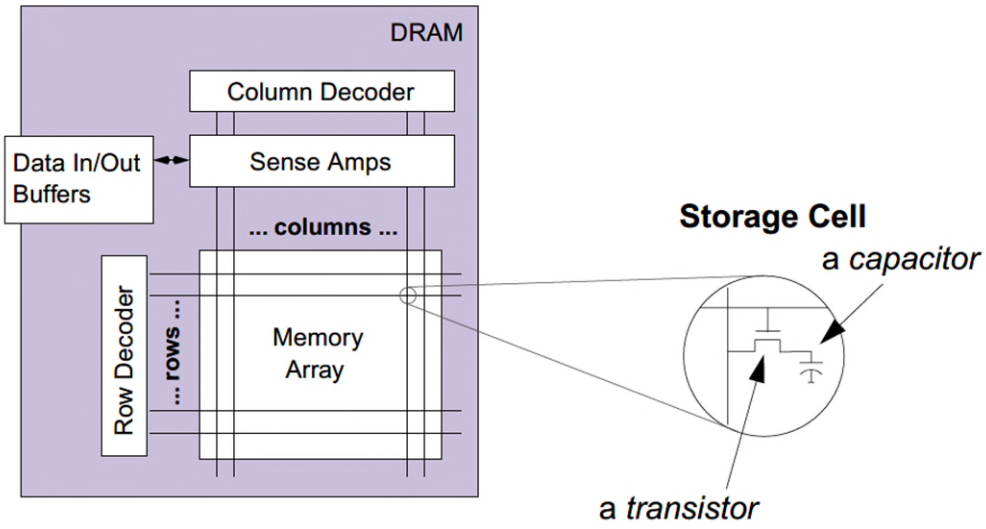


Figure 2: Basic Organization of DRAM Internals
The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a *row* and a *column*.

Insofar as one might argue that "*first group of array dies*" requires multiple slave chips coupled to TSV1, Kim discloses that "any number of … slave chips may be used," EX1014, ¶¶[0048, 0050], consistent with other contemporaneous references (e.g., below) showing multiple groups of stacked dies, where each die in a group is connected to the same data interconnect, EX1024, 9:14-18, Fig.5 (below); EX1003, ¶¶219-220.

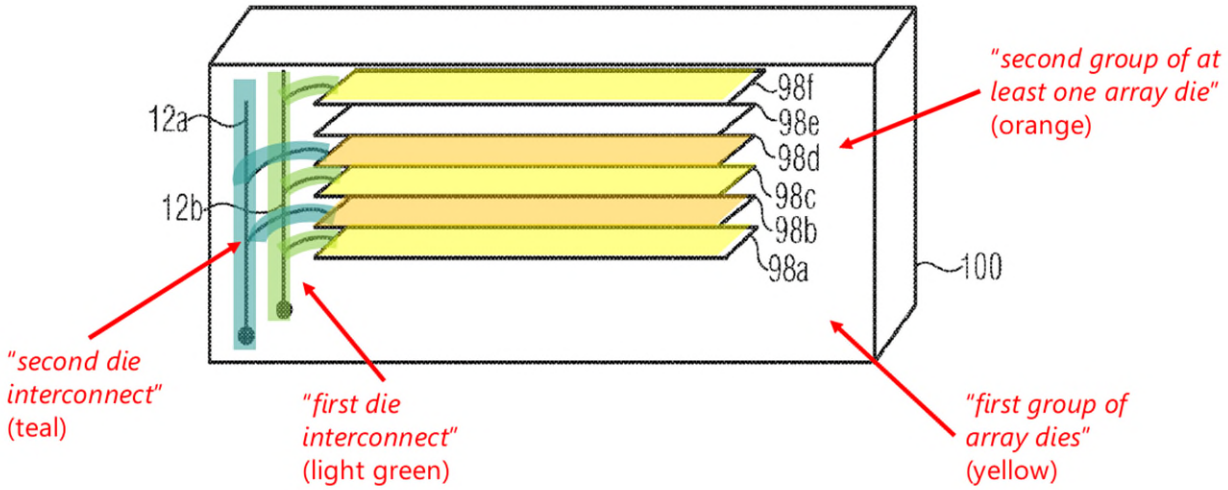


FIG 5

Additionally, Rajan discloses multiple stacked memory chips connected to the same data bus (below), thus further rendering obvious in the combination for Ground 1 that both the "*first*" and "*second*" "*group of array die[s]*" each include multiple "*array dies*" as explained in more detail above (pp.26-30). EX1003, ¶¶221-227.

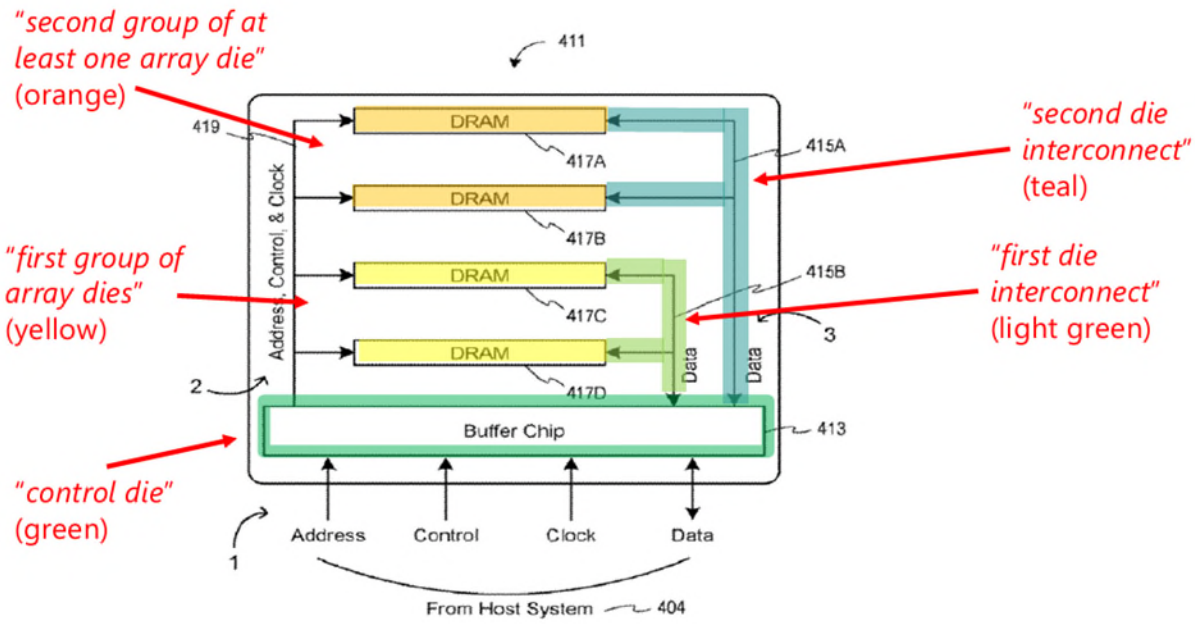
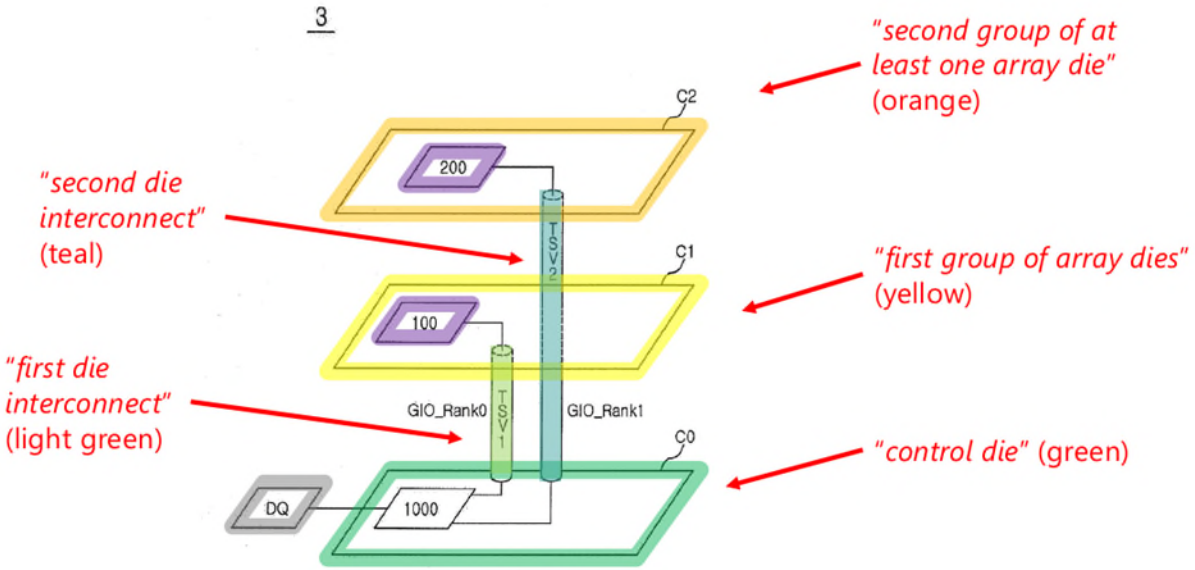


FIG. 4

d) ***[1.d.1]-[1.d.2] Die Interconnects in Electrical Communication with Array Dies***

Ground 1 teaches "*at least a first die interconnect* [e.g., Kim's through-silicon via TSV1] *and a second die interconnect* [e.g., Kim's TSV2], *the first die interconnect in electrical communication with the first group of array dies* [e.g., including Kim's slave chip C1] *and not in electrical communication with the second group of at least one array die* [e.g., including Kim's slave chip C2]," and "*the second die interconnect* [TSV2 is] *in electrical communication with the second group of at least one array die* [including C2] *and not in electrical communication with the first group of array dies* [including C1]; *and*." EX1014, ¶[0049], Fig.5 (below); EX1003, ¶¶230-239.

FIG.5

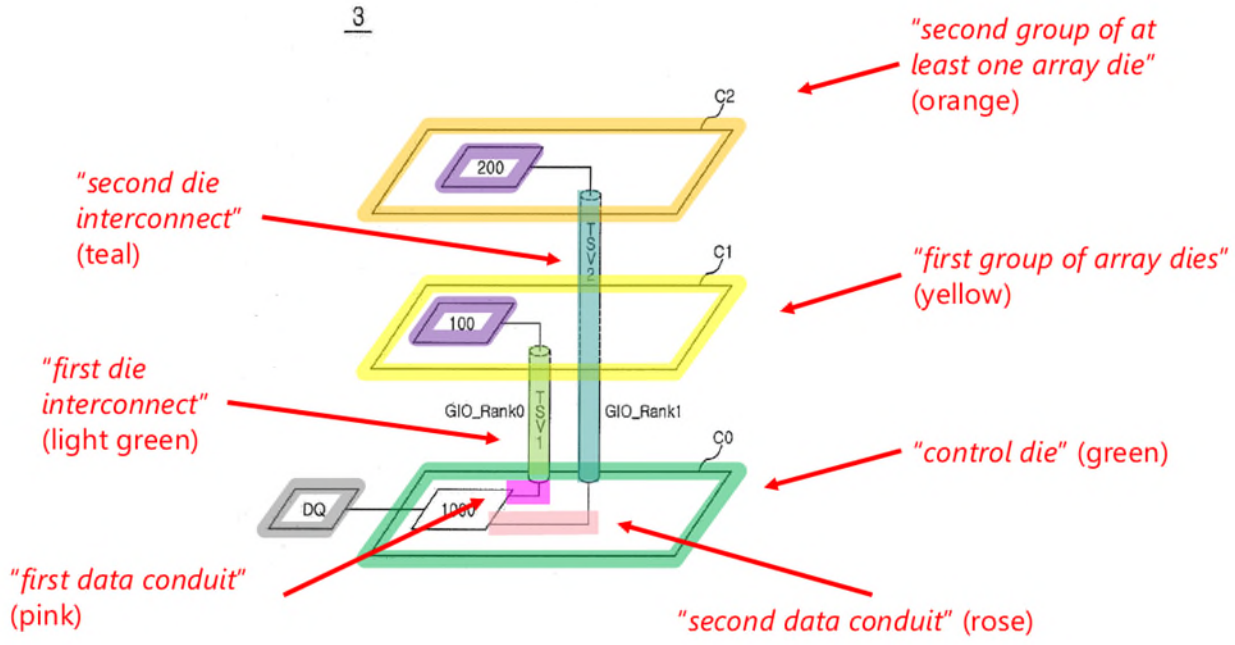


As shown above, TSV1 does not extend up to C2 and thus is not "*in electrical communication*" with C2, while TSV2 passes through C1 without being "*in electrical communication*" with C1 (e.g., there is no data port (purple) or anything else connected to TSV2 in C1). *Id.* Furthermore, a POSITA would have understood from Kim's disclosure that data collisions do not occur because, as illustrated in Figure 5, the data input/output lines through TSV1 and TSV2 are in electrical communication with one and not the other of chip C1 implementing Rank0, and C2 implementing Rank1. EX1014, Abstract, ¶[0045]; EX1003, ¶¶233-237.

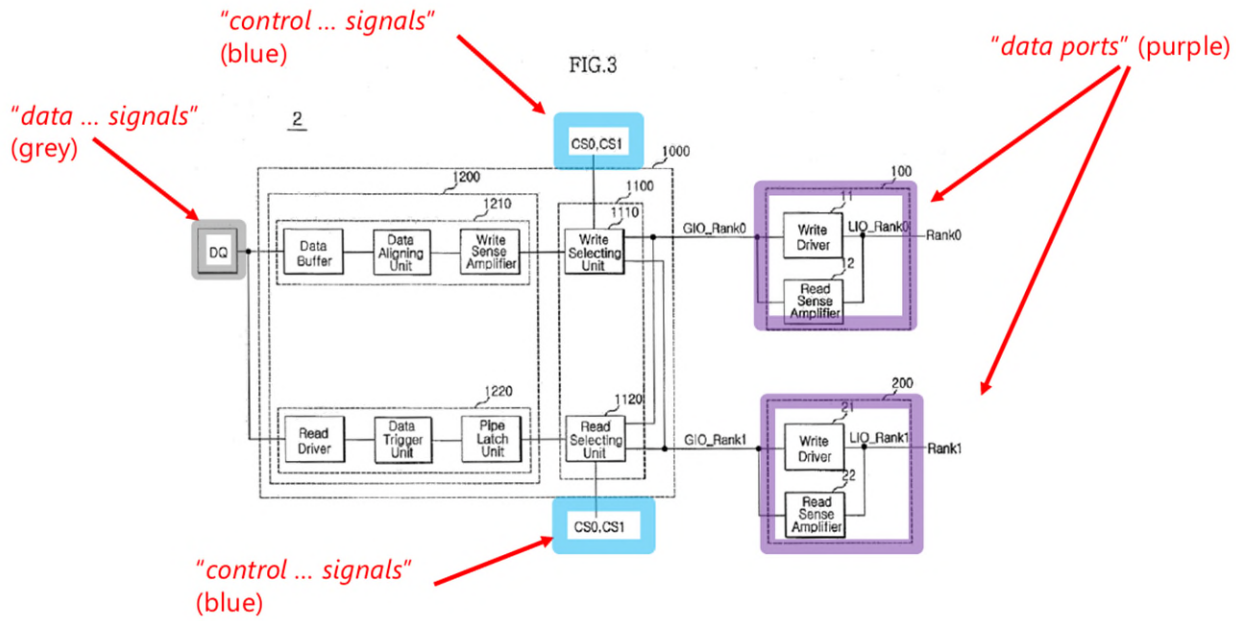
e) ***[1.e.1] Control Die***

Ground 1 teaches "*a control die* [e.g., including Kim's main chip C0 (green)] *comprising*." EX1014, ¶¶[0038, 45], Figs. 3, 5 (below); EX1003, ¶¶240-247.

FIG.5



Kim teaches that the main chip C0 ("*control die*") controls the operation of the memory apparatus, including read/write operations in response to their respective commands from an external device, and that rank selecting unit 1100 (below) in the "*control die*" distinguishes these operations for the first rank (in the "*first group of array dies*") and the second rank (in the "*second group of … array die[s]*"). EX1014, ¶¶[0038, 45], Fig.3 (below); EX1003, ¶¶243-244.

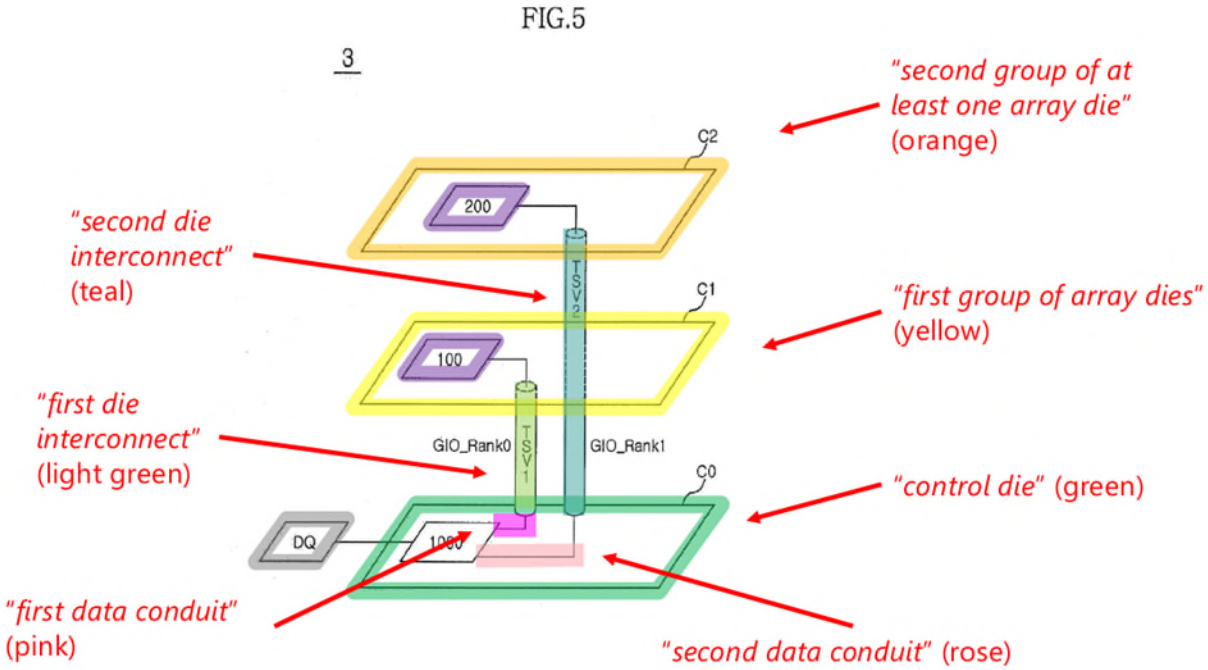


Moreover, the Kim-Rajan combination for Ground 1 (*see* pp.21-30) teaches that the "*control die*" can emulate one or more characteristics (e.g., using rank multiplication, *see* pp.8-11) different from those of the physical memory devices. EX1003, ¶245; EX1015, 6:30-7:67, Fig.18.

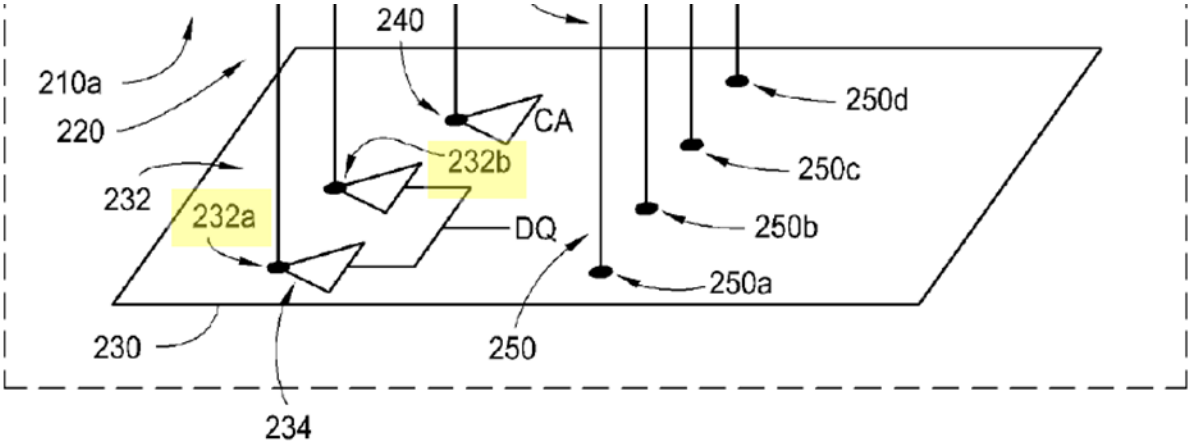
f) ***[1.e.2]-[1.e.3] First and Second Data Conduit***

Kim's Figure 5 (below) shows that Ground 1 teaches "*at least a first data conduit* [including a signal line (pink) for communicating data through data input/output section 1000] *between the first die interconnect* [TSV1 (light green)] *and a first terminal* [e.g., data pad DQ (grey)] *of the plurality of input/output terminals, and at least a second data conduit* [including a signal line (rose) for communicating data through data input/output section 1000] *between the second die interconnect* [TSV2 (teal)] *and the first terminal, the first terminal being a data*

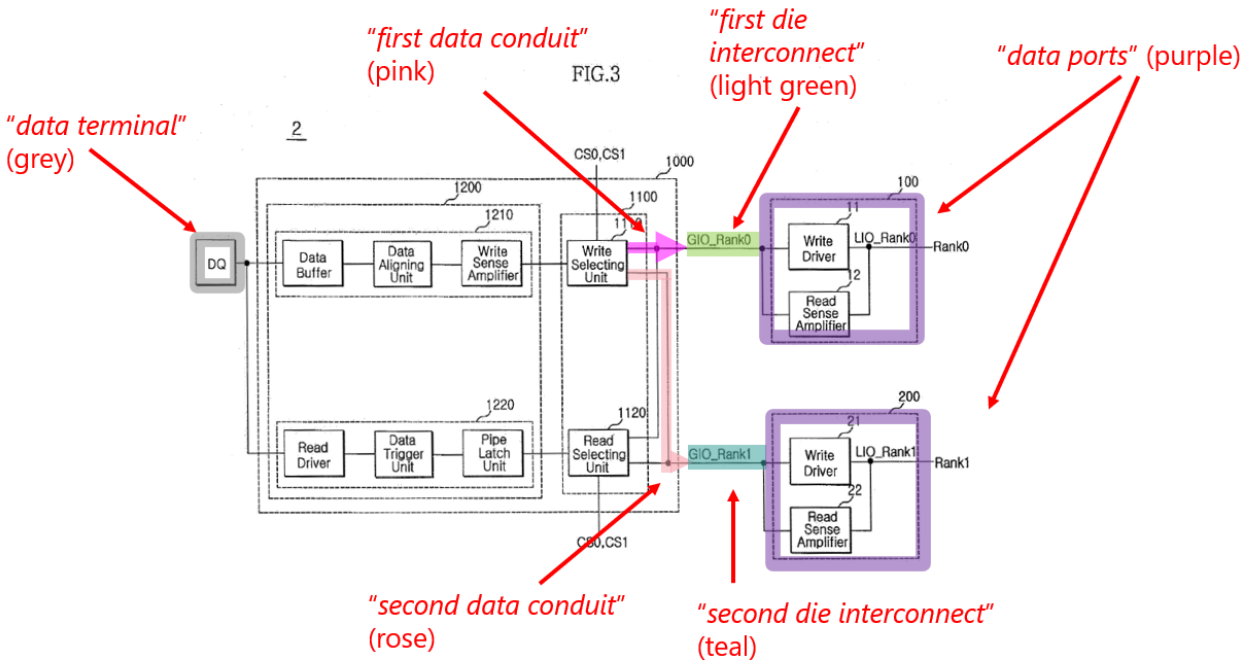
terminal [e.g., data pad DQ (grey)]." EX1014, ¶[0049], Fig.5 (below); EX1003, ¶¶248-264.

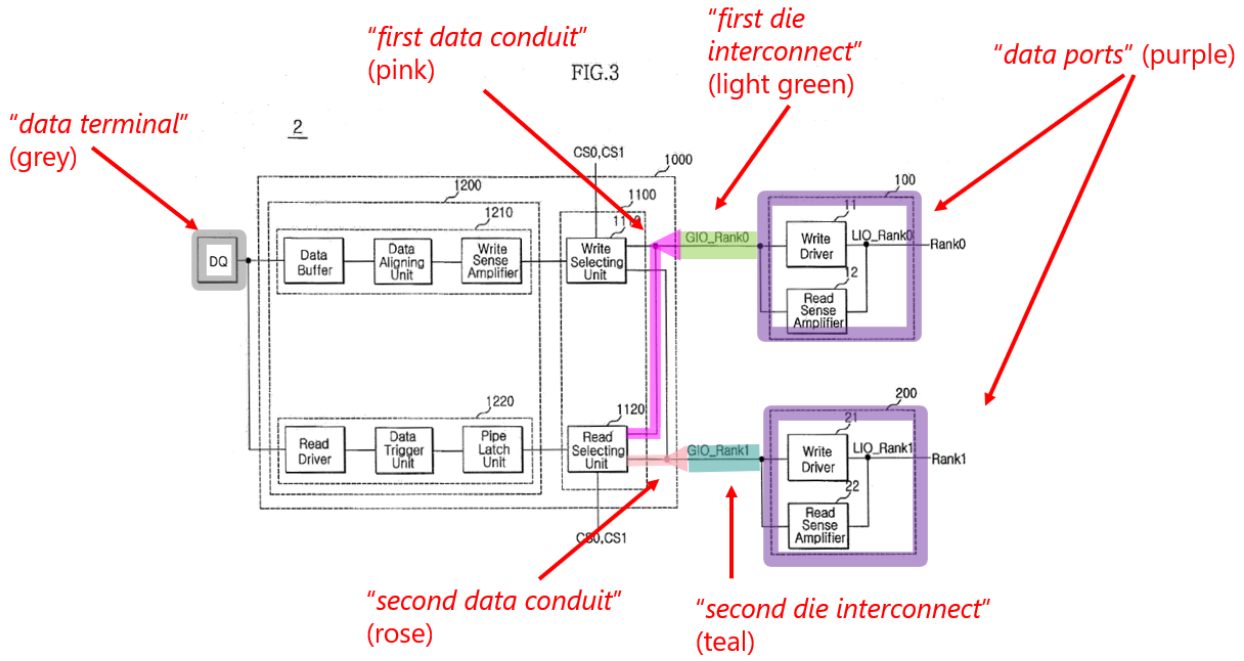


The "*data conduit[s]*" in Kim (above) are similar to the "*data conduit[s]*" 232a and 232b in the 060 Patent (below) that transmit a data signal to a respective die interconnect. EX1001, 6:48-62, 9:28-60, Fig.2 (below in part).



A POSITA would have understood from Kim's description of rank selection by chip selection signals (CS0, CS1) for read/write operations that the "*data conduit*" connecting the write selecting unit 1110 (below) and the read selecting unit 1120 (below) in data input/output section 1000 (above and below) to a TSV to Rank0 is between "*the first die interconnect*," e.g., TSV1, and a "*data terminal*," e.g., data pad DQ (grey, above and below), and the "*data conduit*" connecting the data input/output section 1000 (above and below) to a TSV to Rank1 is between "*the second die interconnect*," e.g., TSV2, and the "*data terminal*," e.g., data pad DQ (grey, above and below). EX1014, ¶¶[0029-30, 0035-38], Fig.3 (first below, showing a first "*data conduit*" (pink) active for write operation to Rank0, or a second "*data conduit*" (rose) active for a write operation to Rank1), and Fig.3 (second below, showing a first "*data conduit*" (pink) active for a read operation from Rank0, or a second "*data conduit*" (rose) active for a read operation from Rank1); EX1003, ¶¶252-261.

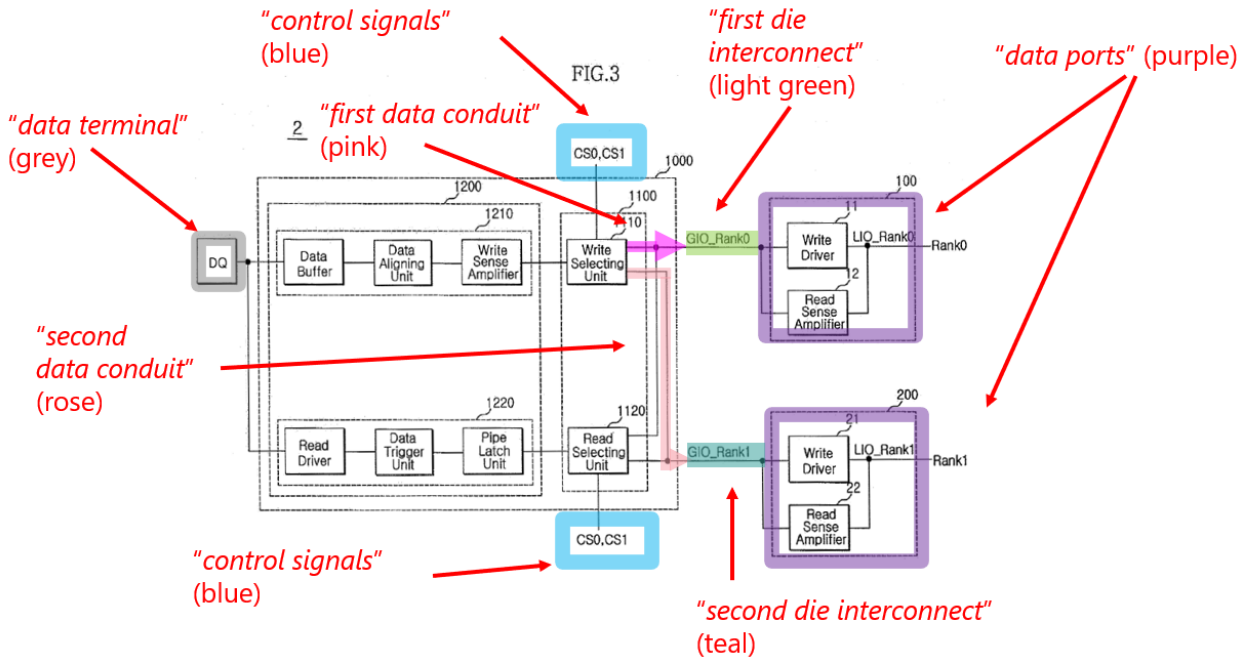


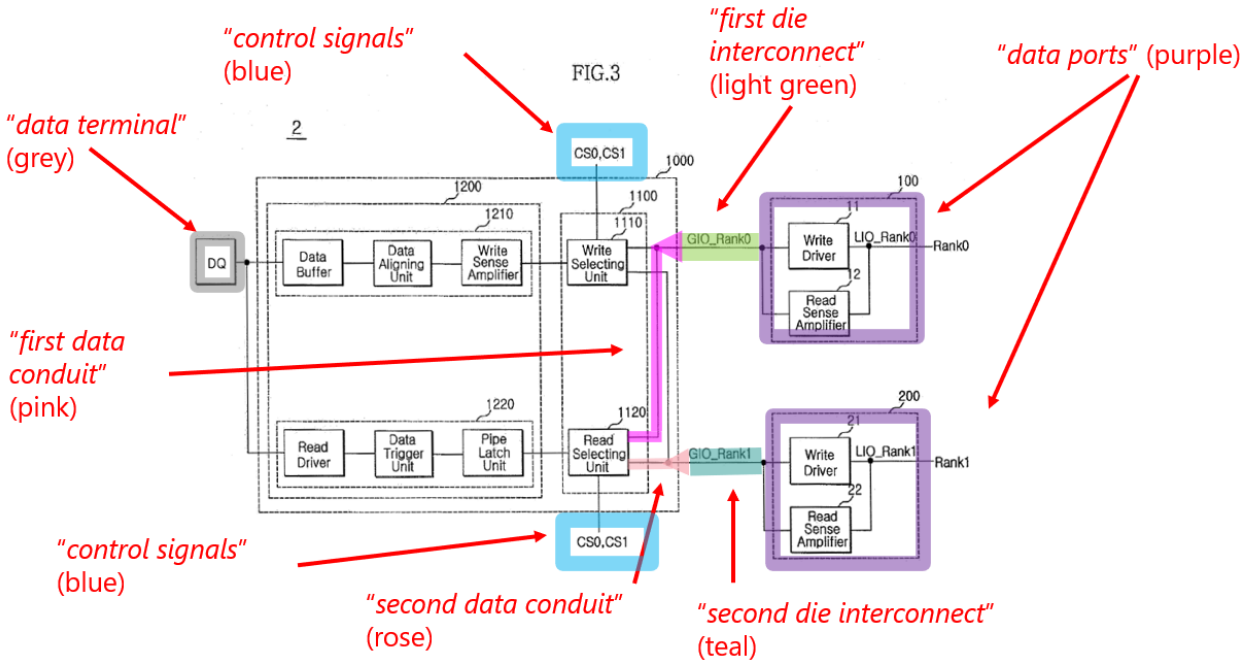


As explained above for claim limitation [1.b] (pp.31-34), Kim discloses that data pad DQ (grey) is a "*data terminal*." EX1003, ¶262.

g) ***[1.e.4] Control Circuit***

Kim's Figure 3 (below, annotated for write (upper) and read (lower) operations) shows that Ground 1 teaches "*the control die* [from [1.e.1], pp.41-42] *further comprising a control circuit* [e.g., in rank selecting unit 1100, including write selecting unit 1110 and read selecting unit 1120] *to control respective states* [e.g., to be active or not active, and if active to transmit data in the read direction or in the write direction] *of the first data conduit* [(pink) to TSV1] *and the second data conduit* [(rose) to TSV2] *in response to control signals* [including chip selection signals CS0 and CS1 and read/write command signals pursuant to the JEDEC standard, EX1019, pp.6-14, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35,] *received via one or more second terminals of the plurality of terminals* [from an external device, as discussed for [1.b], pp.31-34]." EX1014, ¶¶[0032, 0035-36, 0038], Fig.3 (below); EX1003, ¶¶265-272.



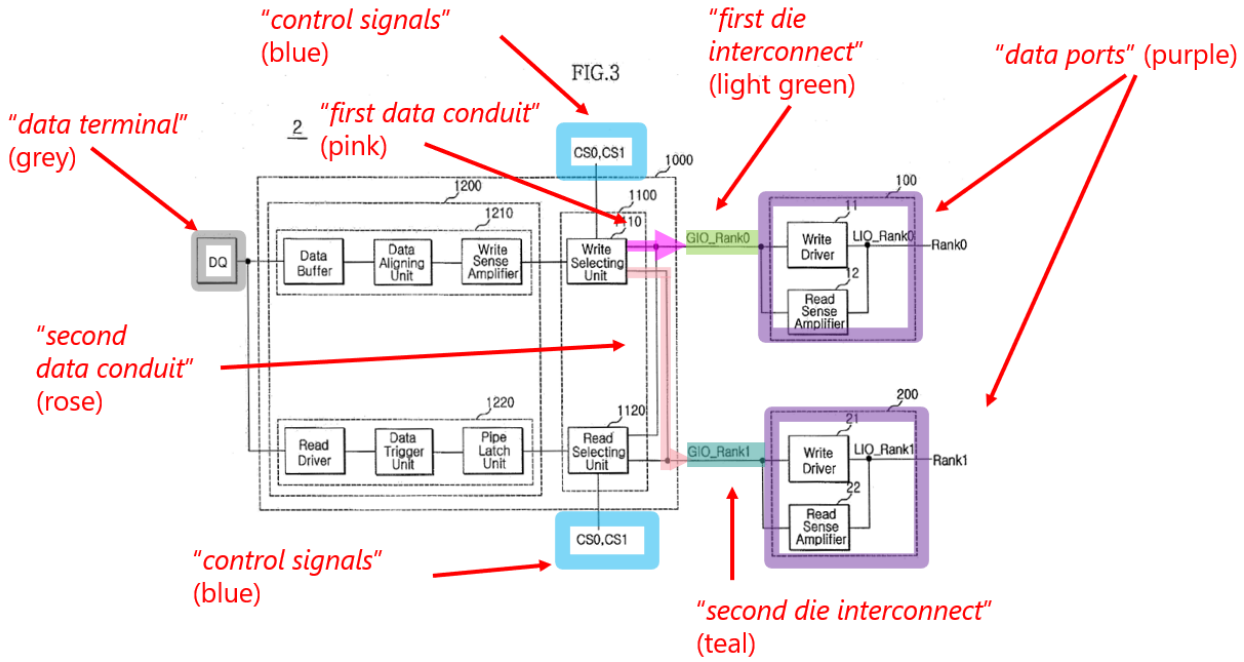


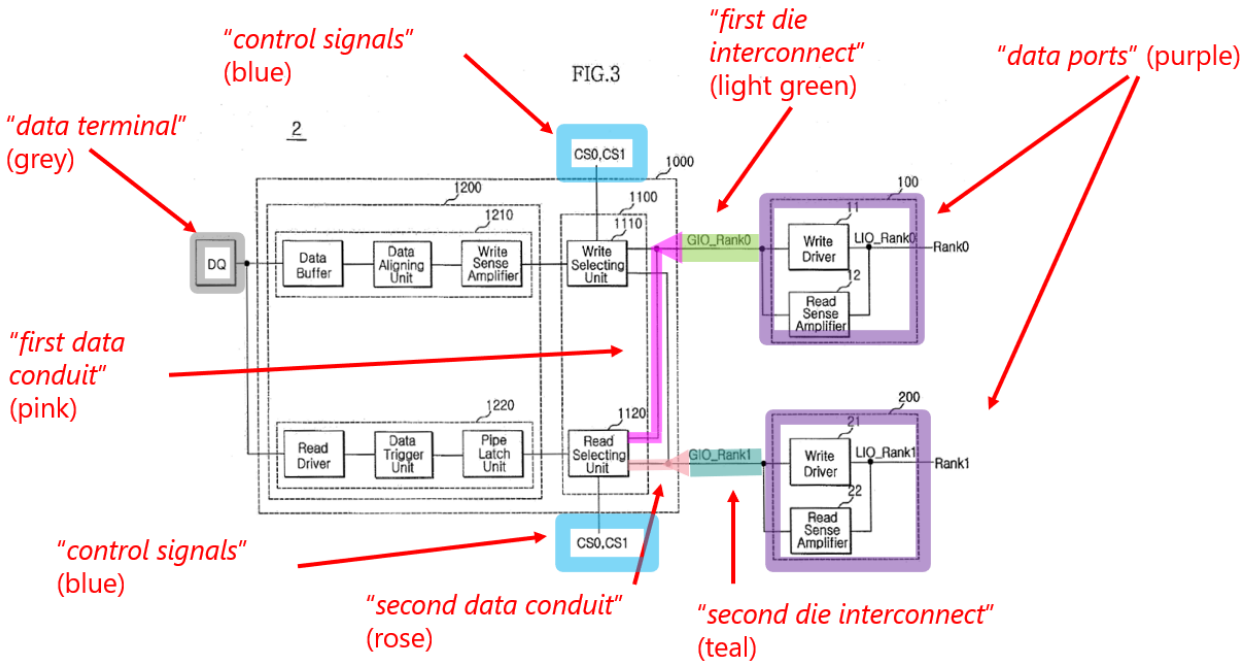
3. Claim 2

Grounds 1 teaches "*claim 1, wherein the control signals* [from the external device] *include data path control signals* [e.g., chip-select and read/write command signals pursuant to the JEDEC standard] *for controlling the first* [(pink)]

and second [(rose)] *data conduits* [including controlling the direction of the data transfer, and the selection of transferring the data through TSV1 or TSV2]."

EX1014, Fig.3 (annotated below for write (upper) and read (lower) operations); EX1003, ¶¶273-280.



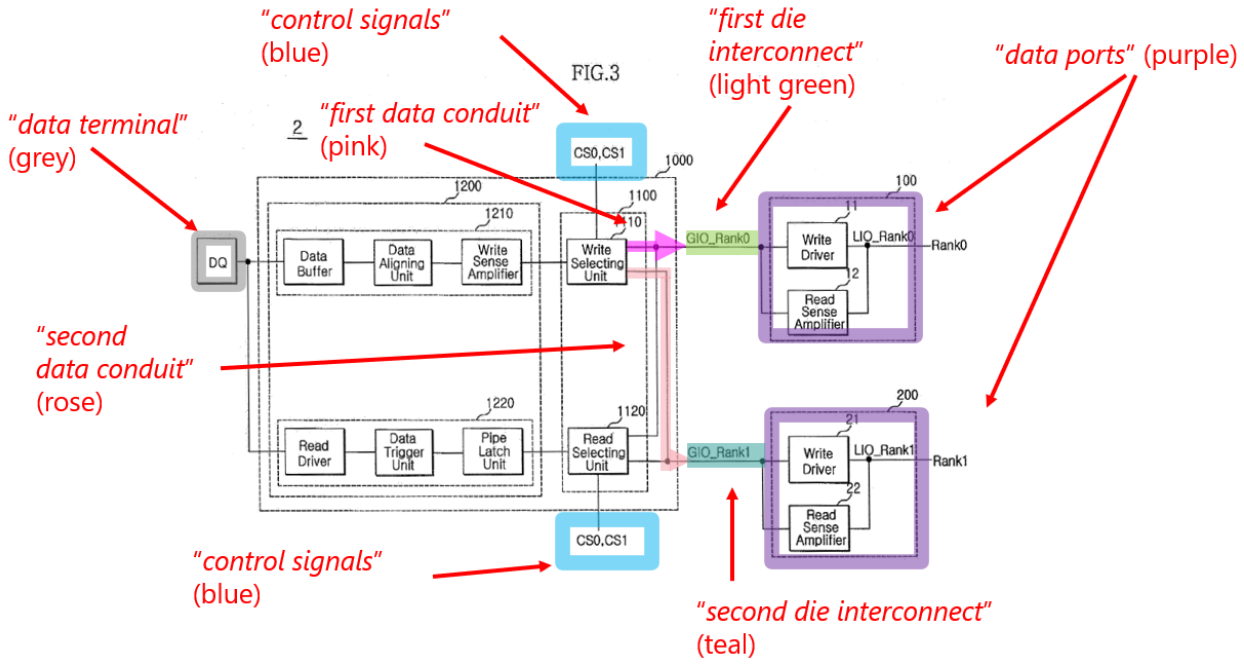


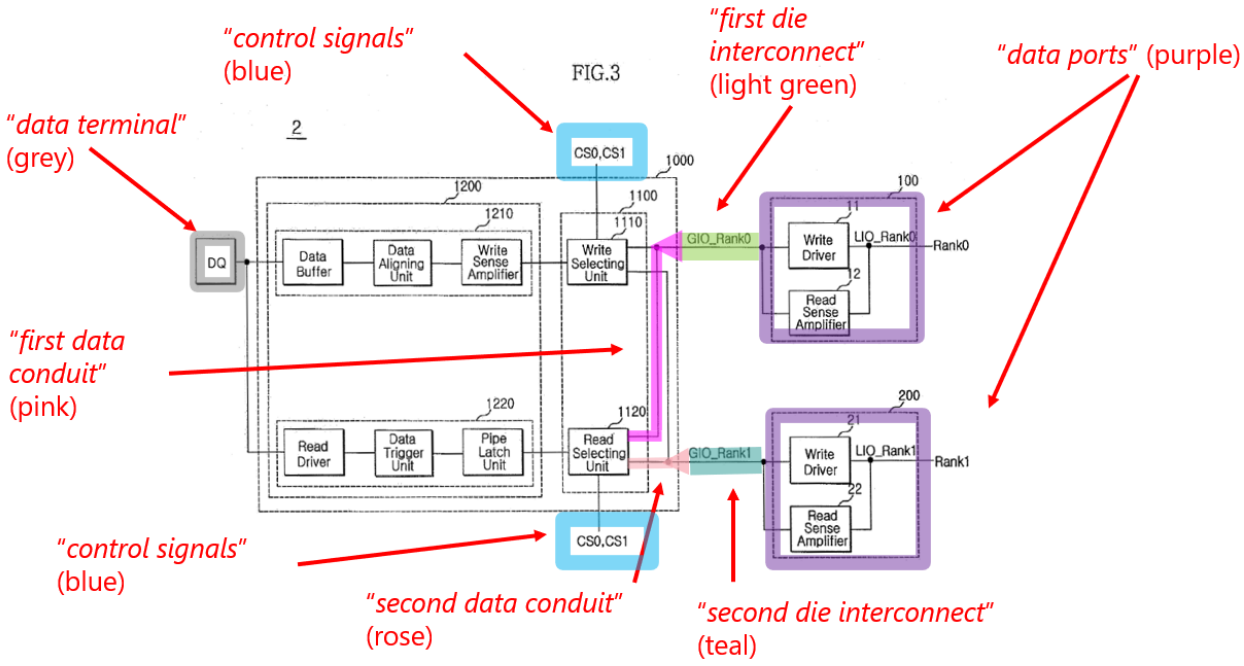
A POSITA would have understood that Kim's chip selection signals and read/write command signals, received by Kim's rank selecting unit 1100 (*see* claim limitation [1.e.4], pp.46-47), are "*data path control signals*" since they determine direction of data transfer (read or write) and select the TSV (TSV1 or TSV2) through which data is transmitted from or to Rank0 or Rank1, respectively. EX1014, ¶¶[0031-38], Fig.3; EX1003, ¶277 (citing ¶¶265-272). Furthermore, Kim teaches that such "*data path control signals*" are needed to avoid collisions. EX1014, ¶[0031]; EX1003, ¶277. Moreover, in the combination of Ground 1, either the "*control circuit*" in the memory package and/or the register on the memory module external to the memory package can implement "rank multiplication," as discussed above (pp.8-11, 28-30), thus affecting the "*data path control signals*." EX1003, ¶278.

4. Claim 3

Ground 1 teaches "*claim 1, wherein the control circuit* [from [1.e.4], pp.46-47, e.g., in Kim's rank selecting unit 1100 (in Fig.3, below)] *is configured to generate data path control signals* [as discussed above for claim 2 (pp.47-49), including "internal write and read signals…[that are] generated," EX1014, ¶[0038]] *for controlling the first and second data conduits* [to or from TSV1 or TSV2] *in response to the received control signals* [including chip selection and JEDEC-standard read/write command signals, from an external device, which may

be "buffered," EX1014, ¶[0038]]." EX1003, ¶¶273-289. As discussed above for claim 2, in the combination of Ground 1, the "*control circuit*" in the memory package can also implement "rank multiplication," as discussed above (pp.8-11, 21-30), thus generating "*data path control signals*." EX1003, ¶287; EX1015, 3:27-30, 6:30-7:67, Fig.18.





5. Claim 4

a) *[4.a] Command/Address Signals*

Ground 1 teaches "*[t]he memory package of claim 3, wherein the control signals include command/address signals* [e.g., "write and read command signals," EX1014, ¶[0038], which, as discussed for claim limitation [1.b] (pp.31-34), and in light of the JEDEC standards, EX1019, pp.6-14, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35, would have been understood by a POSITA to include chip-select (CS) control signals and address signals (e.g., A0-A15) identifying where to store or retrieve the data] *and*." EX1003, ¶¶291-295; *supra* pp.21-30; EX1015, Figs. 4 and 18 (below); *see also* EX1019, p.13 (chip-select control signals are "considered part of the command code").

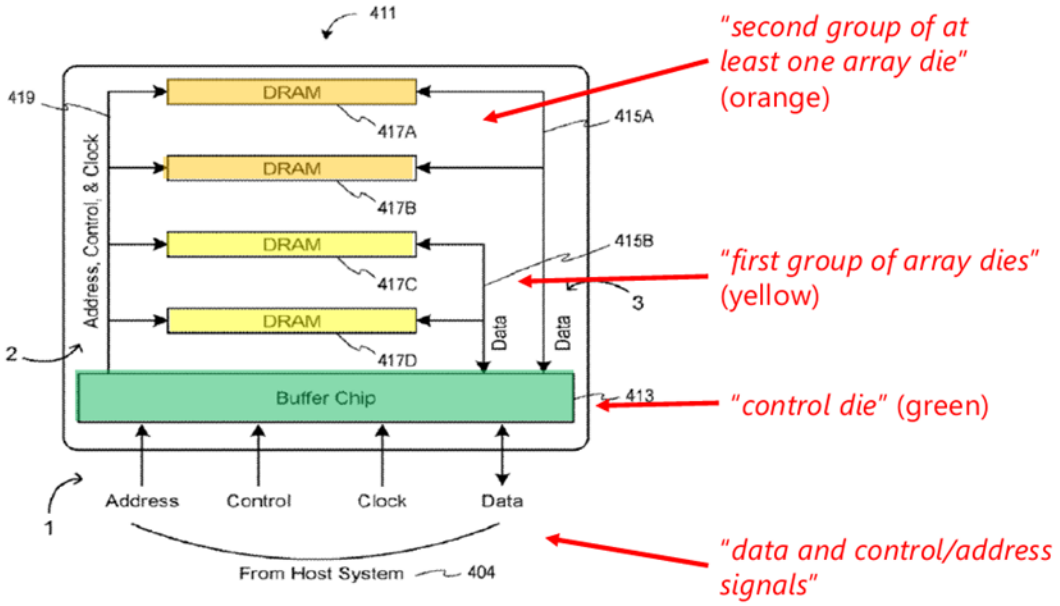

411
419
DRAM
417A
DRAM
417B
DRAM
417C
DRAM
417D
Address, Control, & Clock
415A
415B
3
Data
Data
2
Buffer Chip
413
Address
Control
Clock
Data
1
From Host System
404
"second group of at least one array die" (orange)
"first group of array dies" (yellow)
"control die" (green)
"data and control/address signals"

FIG. 4

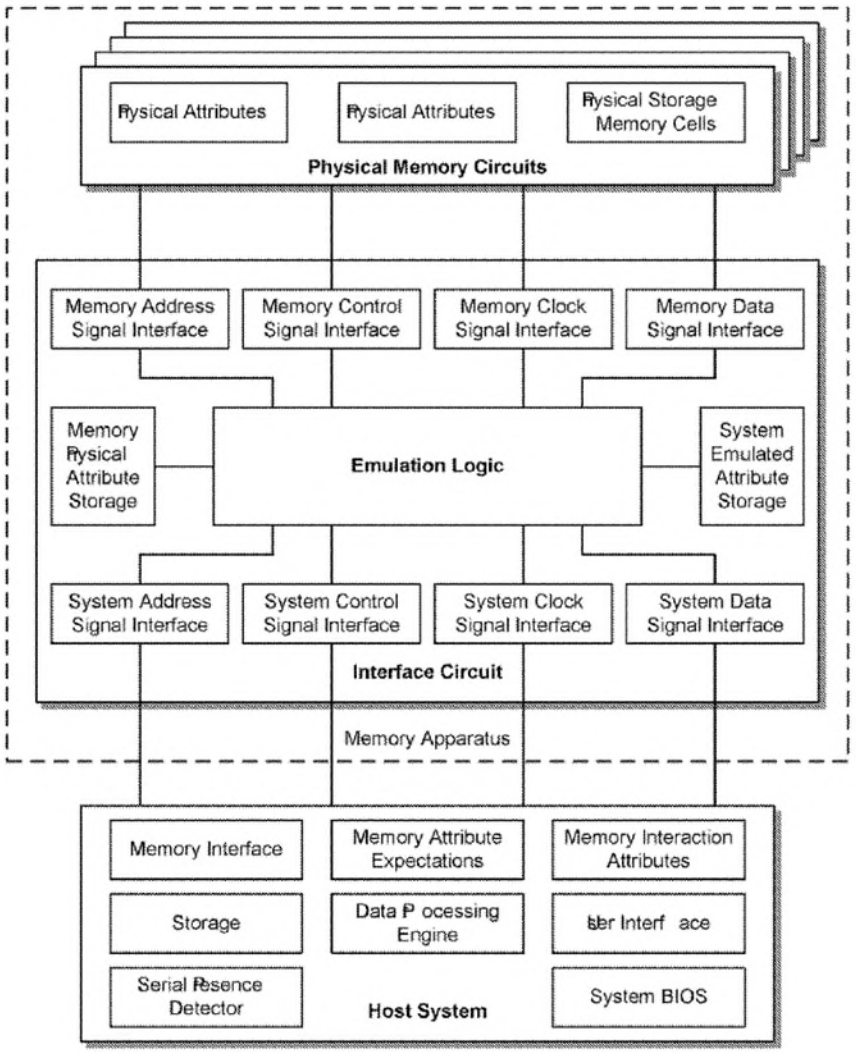


FIG. 18

b) ***[4.b] Control Die Configured to Provide Command/Address Signals***

Ground 1 teaches "*wherein the control die* [from [1.e.1], pp.41-42, e.g., Kim's main chip C0] *is configured to provide the command/address signals* [from [4.a], pp.51-53] *to the plurality of stacked array dies*." EX1003, ¶¶296-307.

Kim teaches that main chip C0 buffers read/write commands, and corresponding address signals, and that C0 provides those buffered signals to the

"*stacked array dies*" enabling those dies to perform the corresponding read and write operations. EX1014, ¶¶[0029-30, 32, 38]; EX1003, ¶¶300-301.

Rajan further makes obvious using a buffer chip ("*control die*," green, below) to provide command/address signals (blue, below), either "altered" (e.g., by rank multiplication) or "unaltered," to the stacked memory chips (yellow and orange, below). EX1015, 14:11-18, 14:55-60, Figs.4, 18 (both below); EX1003, ¶302.

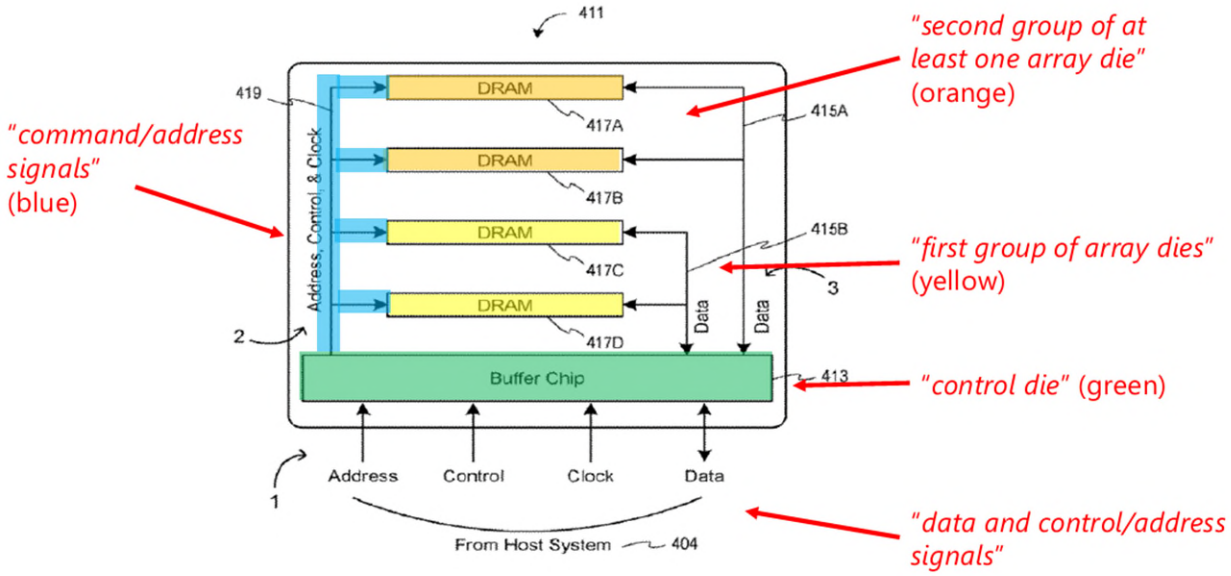


FIG. 4

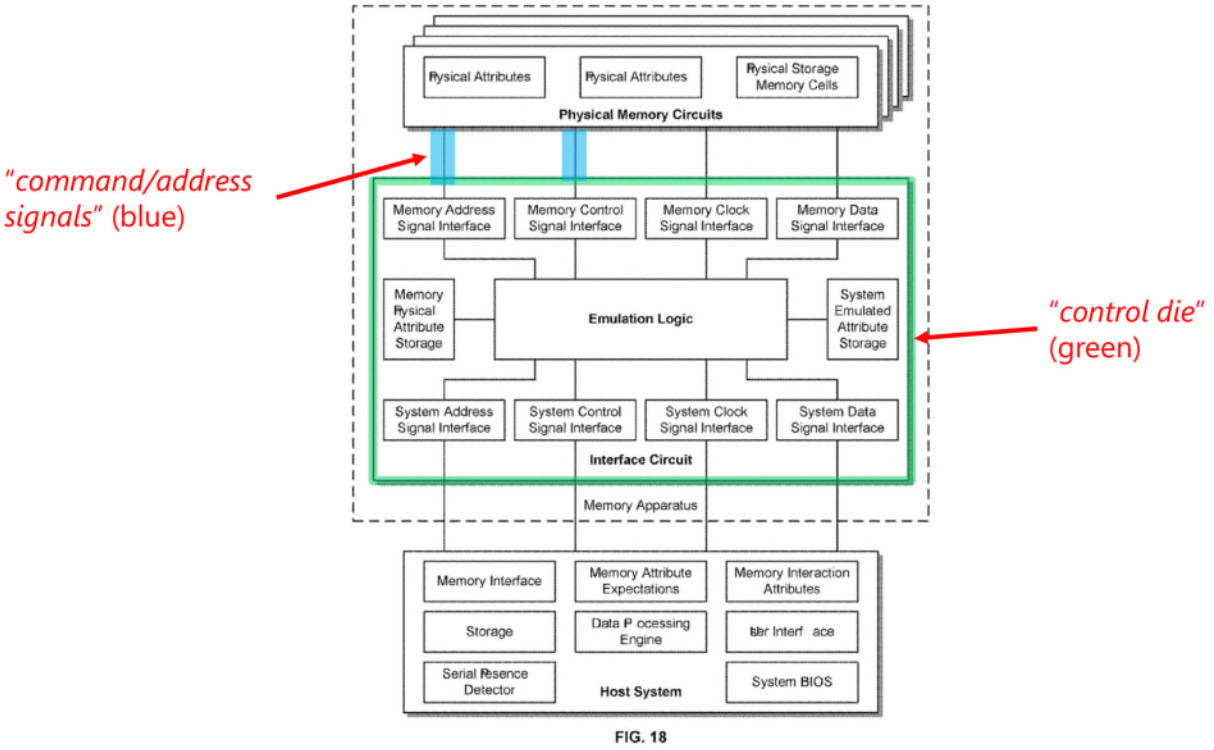
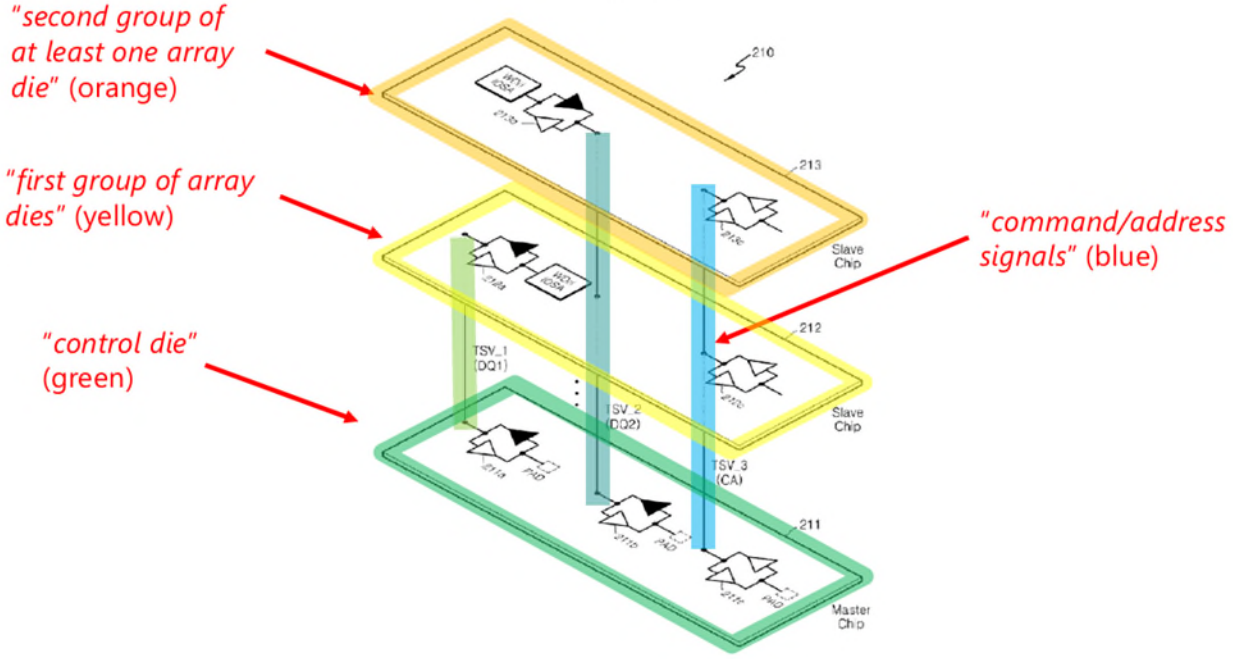
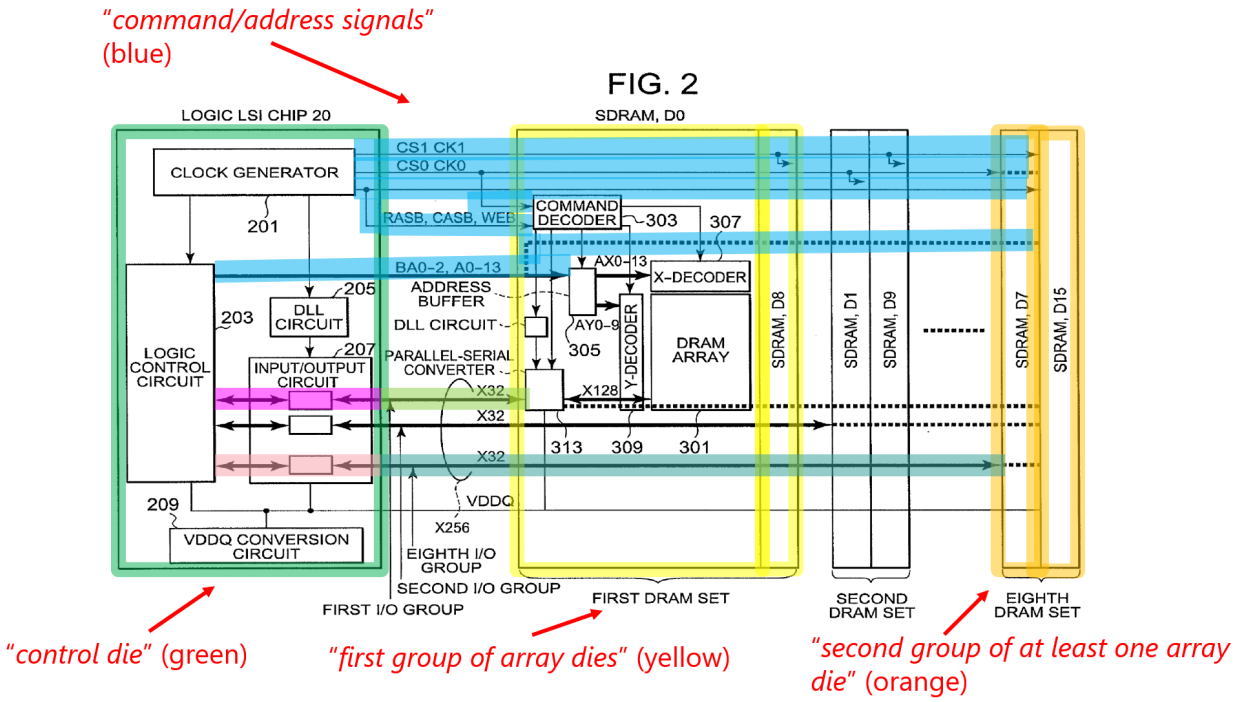


FIG. 18

Furthermore, a POSITA would have been motivated to provide the command/address signals to the stacked memory chips given that it was a technique commonly used at the time, as demonstrated by, e.g., Figures 1A and 1B of the 060 Patent (as admitted prior art), EX1001, 1:39-42, 2:5-8, Figs.1A-1B; other contemporaneous references such as Lee (first below) and Riho (second below), EX1034, Fig.22A (first below); EX1016, ¶¶[0038, 0043], Fig.2 (second below); and the JEDEC standard, EX1019, pp.13, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35, resulting in nothing more than expected: having the address and command signals available at each memory chip. EX1003, ¶¶303-305.

FIG. 22A

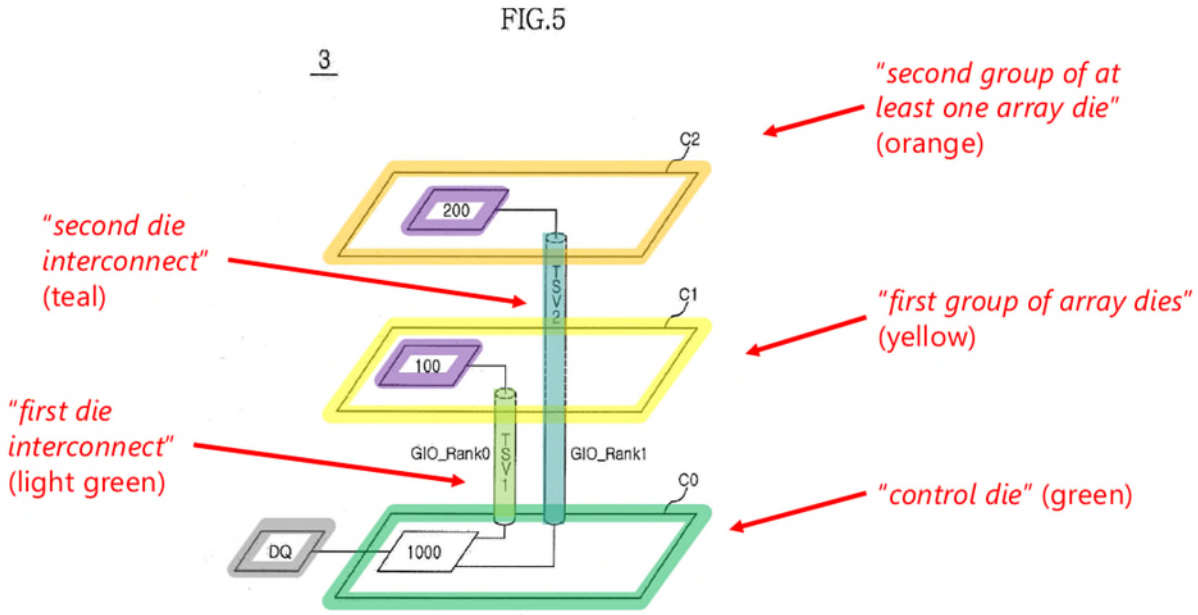




6. Claim 5

Ground 1 teaches "*[t]he memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via* [TSV1 (light green)] *and*

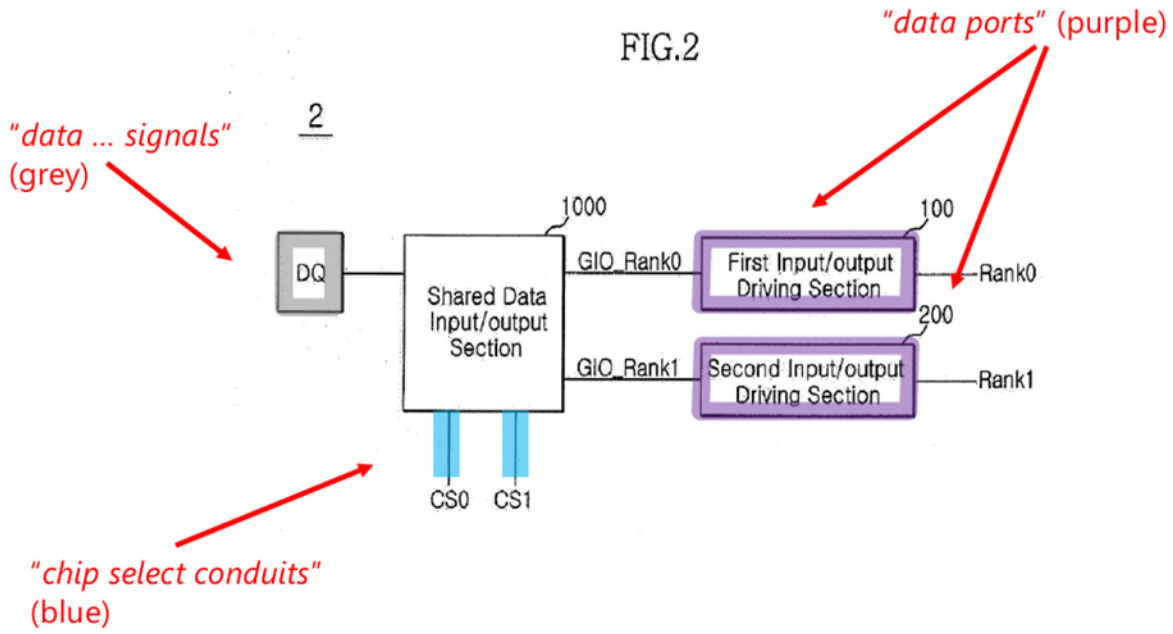
wherein the second die interconnect comprises a second through-silicon via [TSV2 (teal)]." EX1014, ¶¶[0046-49], Fig.5 (below); EX1003, ¶¶308-313.



7. Claim 6

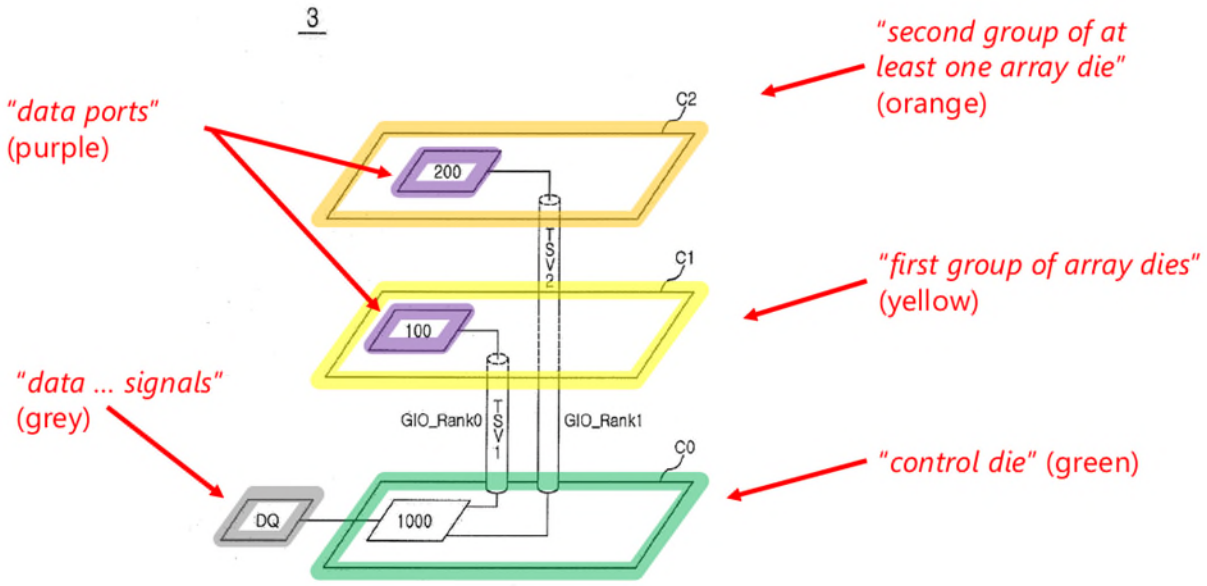
a) *[6.a] Chip-Select Conduits*

Ground 1 teaches "*[t]he memory package of claim 1, wherein the control die* [from [1.e.1], pp.41-42, e.g., Kim's main chip C0] *further comprises chip-select conduits* [(blue) for conducting chip-select signals like CS0 and CS1]*, the memory package further comprising*." EX1014, ¶[0028, 0032], Fig.2 (below); EX1003, ¶¶315-323.



The "chip-select bus … is essential in a JEDEC style memory system." EX1022, p.319; EX1023, pp.2-4, 9, Fig.16. A POSITA would have understood from Kim's description of the generation of chip-select signals CS0 and CS1 (above), which may be internal signals, and of data transmission during read and write operations, that the main chip C0 ("*control die*"), including the shared data input/output section 1000 (above and below), buffers CS0 and CS1 and includes "*chip-select conduits*" to conduct buffered CS0 and CS1 to other parts of the stack. EX1014, ¶¶[0028, 32], Fig.5; *see also* pp.71-73 (explaining for claim 12 that the chip-select signal is received at the bottom surface of the "*control die*" and provided to the top surface); EX1003, ¶¶318-319.

FIG.5



Moreover, in the combination of Ground 1, it would be obvious to use "*chip-select conduits*" to transmit generated chip-select signals to corresponding die-interconnects as part of "rank multiplication." *Supra* pp.8-11, 28-30; EX1015, 3:27-30, 6:30-7:67; EX1003, ¶320. Furthermore, a POSITA would understand that a "buffer chip," as also disclosed by Rajan, included drivers (e.g., in the "*chip-select conduits*") to properly transmit the chip-select signals from the "*control die*" to the respective "*array dies*." *Id.*; EX1003, ¶321.

b) ***[6.b] Third Die Interconnects***

Ground 1 teaches "*third die interconnects* [e.g., between main chip C0 and slave chips C1, C2, to couple buffered chip-select signals CS0, CS1 from main chip C0 to slave chips C1 and C2, respectively, to perform read/write operations] *coupled between respective chip-select conduits and respective ones of the*

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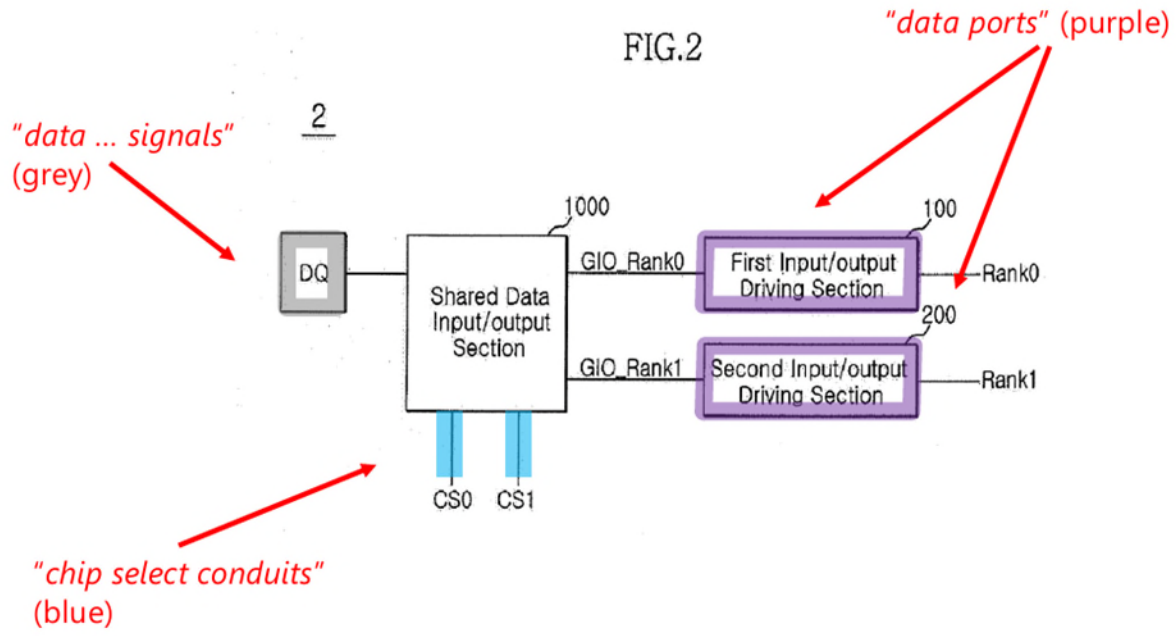
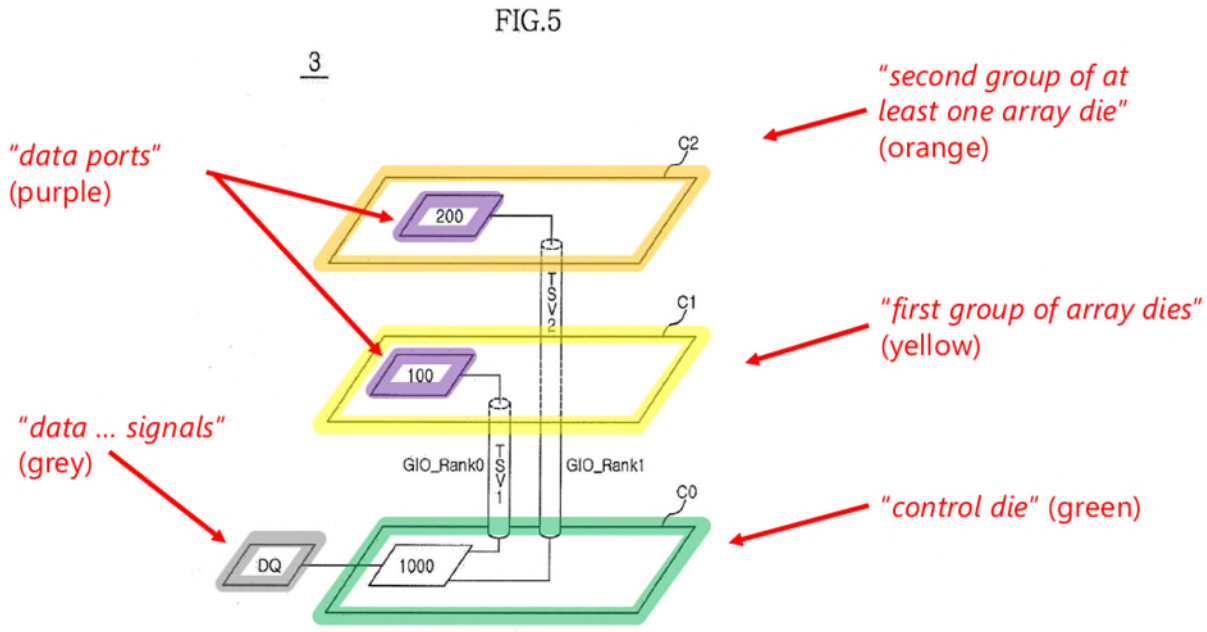
plurality of stacked array dies." EX1014, ¶¶[0029-30, 0049], Figs.2, 5 (below); EX1003, ¶¶324-334.





It would be obvious in light of Kim's disclosure above to include "*third die interconnects*" for the chip-select signals to enable read/write operations by the

"*array dies*." EX1003, ¶¶327-328. Indeed, the "chip-select bus … is essential in a JEDEC style memory system," EX1022, p.319; EX1023, pp.2-4, 9, Fig.16, and the JEDEC standard required separate chip-select signals for each stacked memory chip (below, red), EX1019, pp.12-13, Fig.2 (below); EX1003, ¶330.

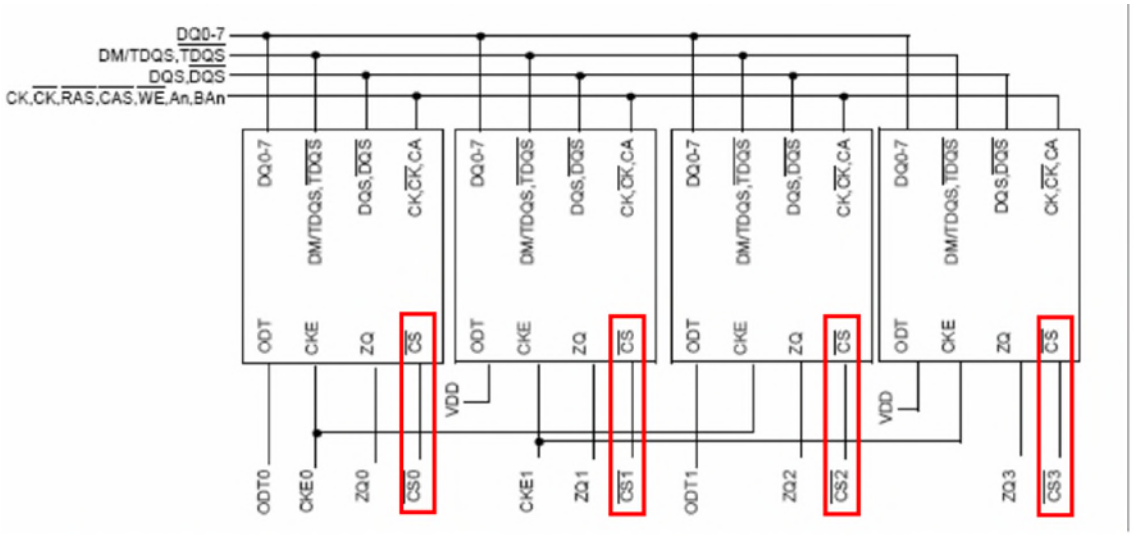


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

Rajan (in the combination of Ground 1, pp.21-30) further renders obvious "*third die interconnects*" for the chip-select signals by teaching that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack." EX1015, 6:34-38, Fig.4 (below); EX1003, ¶¶329-330.

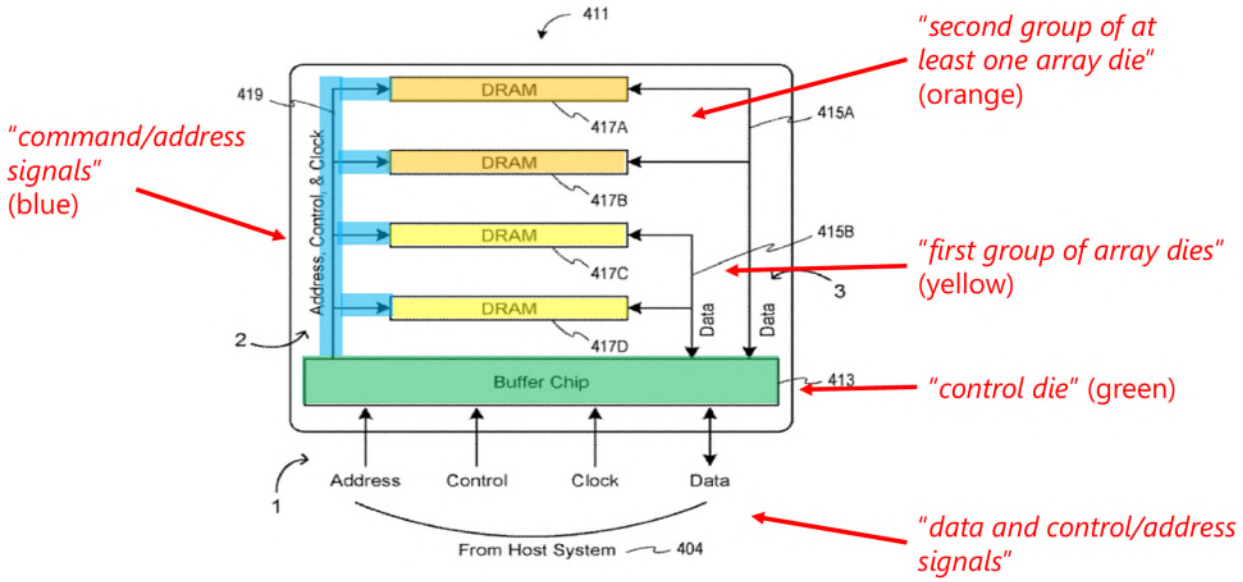


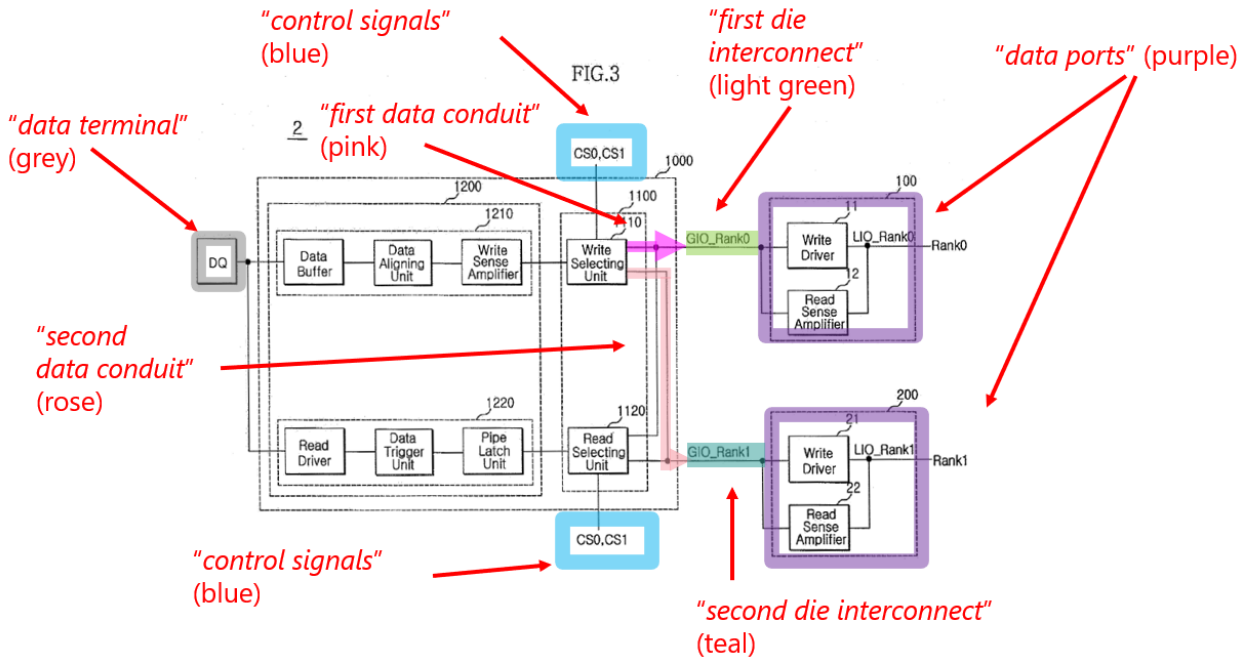
FIG. 4

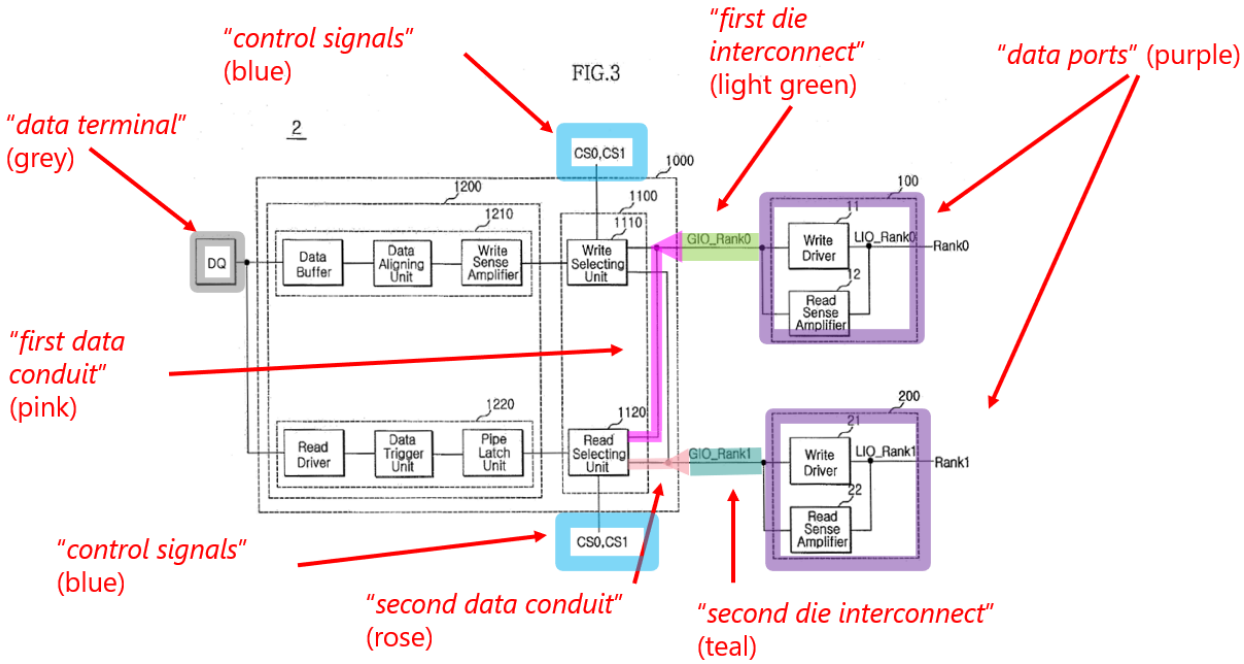
Other references, including Riho and the admitted prior art in the 060 Patent, further confirm that transmitting chip-select signals through die interconnects to select a chip in the stack was well-known and within the level of skill at the time. EX1016, ¶[0038]; EX1001, 1:49-56, Figs.1A-1B; EX1003, ¶¶331-332.

8. Claim 8

a) *[8.a] Data Path Control Signals*

Ground 1 teaches "*[t]he memory package of claim 1, wherein the respective states of the first data conduit* [(pink, connected to TSV1)] *and the second data conduit* [(rose, connected to TSV2)] *are controlled by one or more data path control signals* [e.g., the chip-select and read/write command signals, as explained for claims 2-3 (pp.47-51)]." EX1014, Fig.3 (below, annotated for write (upper) and read (lower) operations); EX1003, ¶¶352-356.





b) ***[8.b] Control Die***

(1) [8.b.1] Control Die is Configurable

Ground 1 teaches "*wherein the control die* [from [1.e.1], pp.41-42] *is configurable to operate in any one of a first mode* [e.g., when the number of ranks

seen by the host system equals the number of ranks actually in the stack, *see* [8.b.2] below] *and a second mode* [e.g., when Rajan's interface (below) implemented in Kim's main chip C0 emulates an interface with fewer ranks than are actually in the stack, *see* [8.b.3] below]*, and wherein*." EX1015, 14:51-62, Fig.18 (below); EX1003, ¶¶357-364.

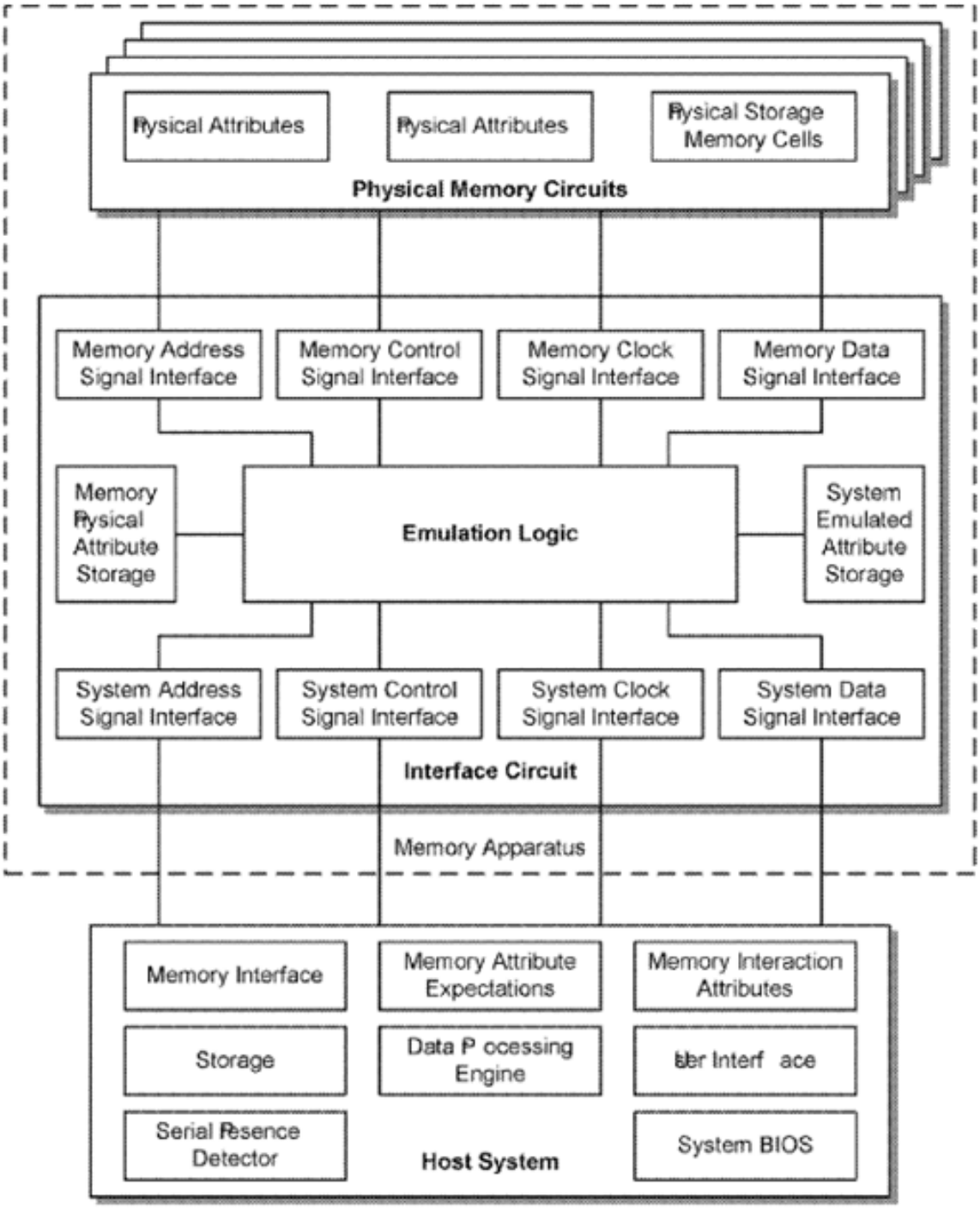


FIG. 18

A POSITA would have been motivated to implement Rajan's different modes of interface operation to make Kim's memory stack compatible with host

systems having different memory attribute expectations and memory interaction attributes. *Supra* pp.21-30; EX1015, Abstract, Fig.18; EX1003, ¶362.

(2) [8.b.2] First Mode

As explained for claim 2 (pp.47-49), Ground 1 teaches "*in the first mode, the control die receives the data path control signals* [e.g., Kim's chip selection signals CS0, CS1 and read/write commands] *from the one or more external devices; and*." EX1003, ¶¶365-369.

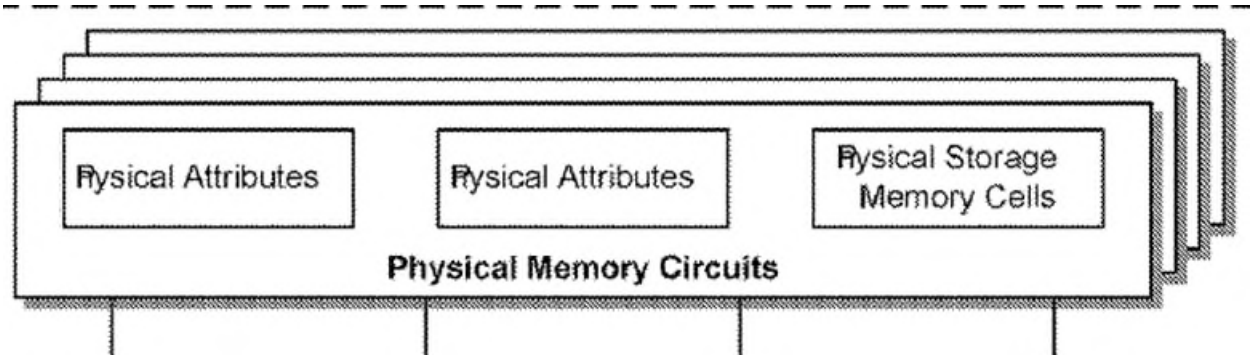
(3) [8.b.3] Second Mode

Ground 1 teaches "*in the second mode* [e.g., when Rajan's interface implemented in Kim's main chip C0 emulates an interface with fewer ranks, e.g., to allow it to operate with systems having different attribute requirements ("rank multiplication"), *see supra* pp.8-11, 63-66]*, the control die generates the data path control signals* [e.g., chip-select signals as explained for claim 2 (pp.47-49)] *from at least some of the control/address signals received from the one or more external devices* [e.g., by using the most significant address bit to generate additional chip-select signals, EX1015, 7:4-67]." EX1003, ¶¶370-376.

9. Claim 9

Ground 1 teaches "*[t]he memory package of claim 1, wherein the control die* [from [1.e.1], pp.41-42] *further comprises command/address conduits* [e.g., conduits for the command/address signals discussed for claim 4, pp.51-56] *configured to provide corresponding command/address signals to the array dies*

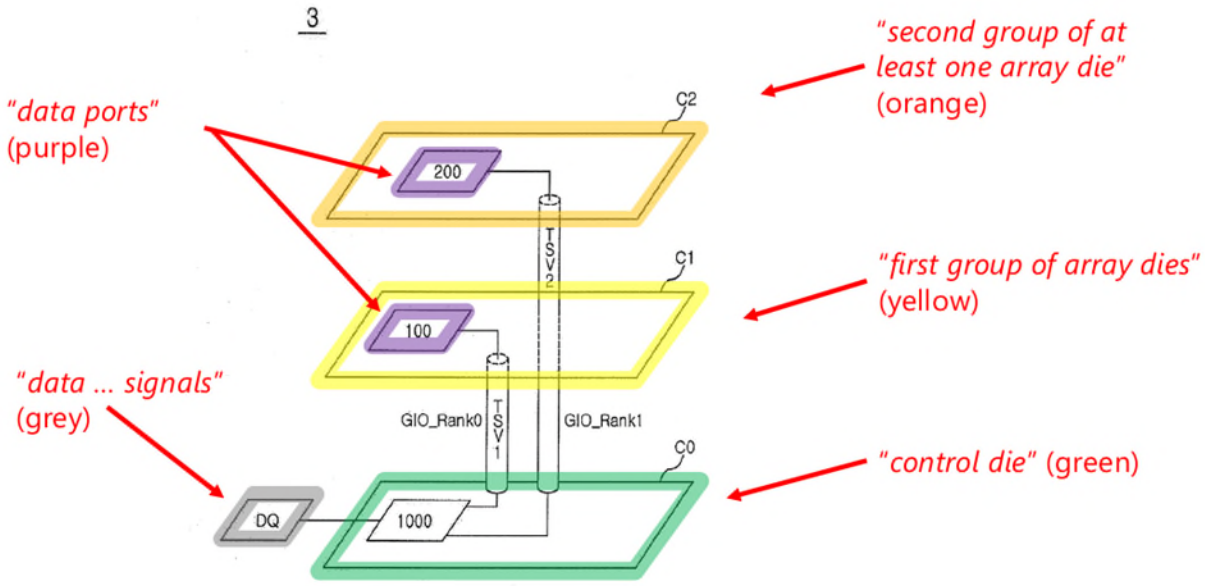
[in Kim's memory device stack in view of Rajan, as discussed for claim 4, pp.49-54, and [1.b]-[1.c], pp.31-39]; *the command/address signals including at least one memory cell address* [*see id.*; EX1019, p.13 ("A0-A15"); EX1015, 6:46-49, Fig.18 (below, illustrating Physical Memory Circuits including Physical Storage Memory Cells)]." EX1003, ¶¶377-387.



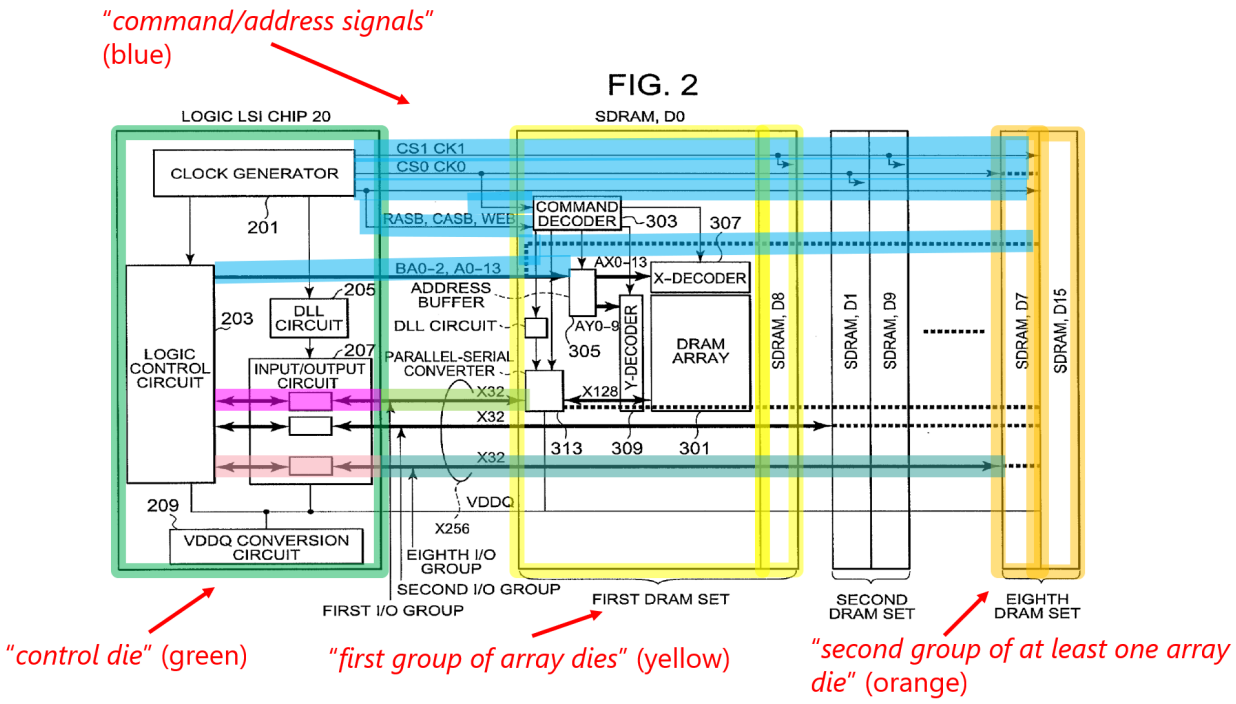
10. Claim 10

Ground 1 teaches "*[t]he memory package of claim 1, wherein the control die* [from [1.e.1], pp.41-42] *further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies* [to power the operation of the memory chips (yellow, orange) and drivers in the data ports (purple), including read/write operations]." EX1014, ¶[0026], Fig. 5 (below); EX1003, ¶¶388-396.

FIG.5



Other contemporaneous references, like Riho (below), also provided a motivation to supply power to the "*array dies*" to perform the operations of storing, amplifying, and transmitting data. EX1016, ¶[0036] (describing VDDQ conversion circuit 209), Fig.2 (below); EX1003, ¶393. A POSITA would have understood that a "*supply voltage*," e.g., VDDQ, would also require a corresponding "*ground signal*" to close the circuit, as standardized by JEDEC, EX1019, p.14. EX1003, ¶394.



11. Independent Claim 11

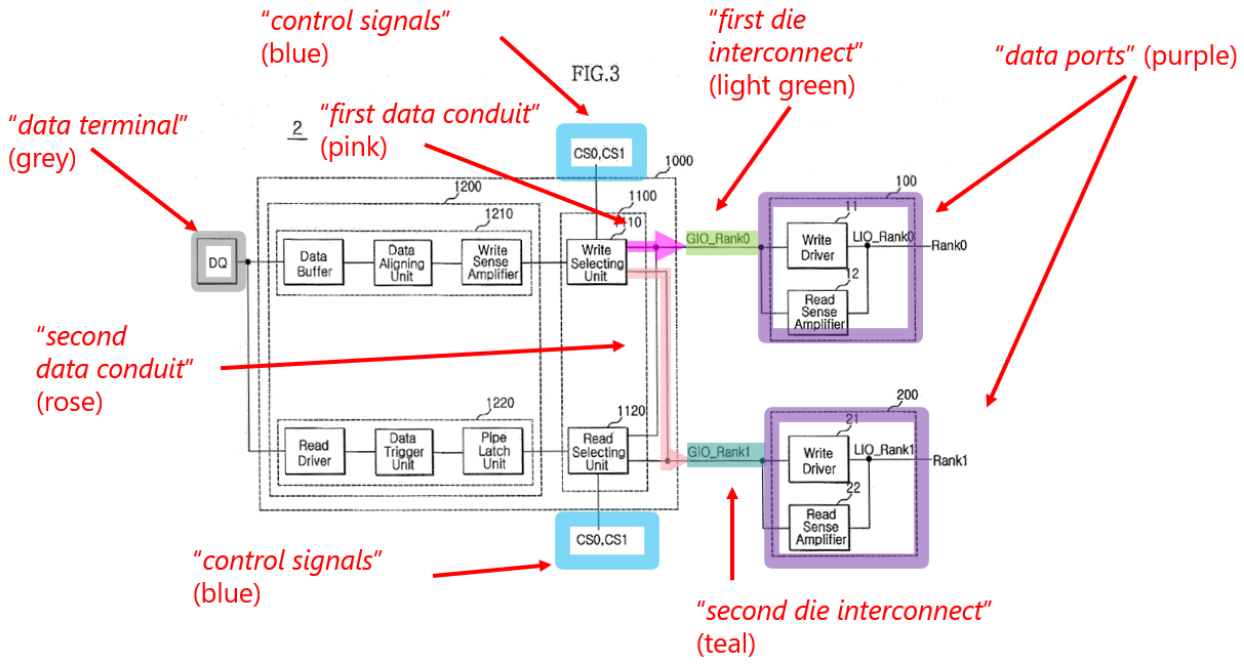
The limitations of claim 11 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[11.a]	[1.a]	¶¶398-400 (¶¶184-188)
[11.b]	[1.b]	¶¶401-404 (¶¶189-210)
[11.c]	[1.c]	¶¶405-408 (¶¶211-229)
[11.d.1]-[11.d.2]	[1.d.1]-[1.d.2]	¶¶409-412 (¶¶230-239)
[11.e.1]	[1.e.1]	¶¶413-416 (¶¶240-247)

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[11.e.2]-[11.e.3]	[1.e.2]-[1.e.3][2]	¶¶417-420 (¶¶248-264)
[11.e.4]	[6.a]-[6.b]	¶¶421-424 (¶¶315-334)
[11.e.5]	[1.e.4] and directly below	¶¶425-434 (¶¶265-272)

For [11.e.5], Ground 1 further teaches "*driv[ing] a data signal* [e.g., by Kim's data input part 1210, through write selecting unit 1110] *to an array die* [e.g., in Rank0 or Rank1] *selected by at least one of the chip-select signals*," *see* EX1014, ¶¶[0035, 40], Fig.3 (annotated below), even insofar as one may argue this requires a separate driver for each of the first and second data conduits, as explained below for [15.a] (pp.87-88). EX1003, ¶¶429-431.

[2] As explained below for [15.a] (pp.87-88), it would also be obvious for the first and second data conduits to each include a respective driver. EX1003, ¶¶456-464.

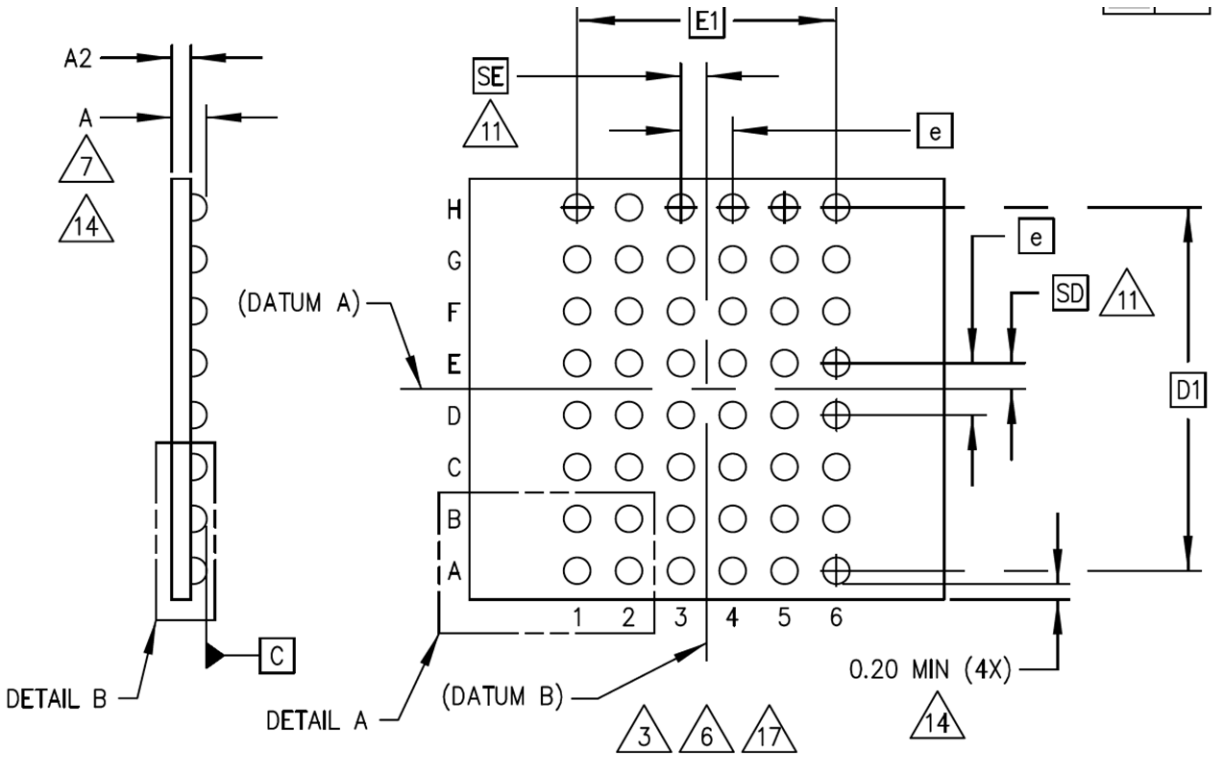


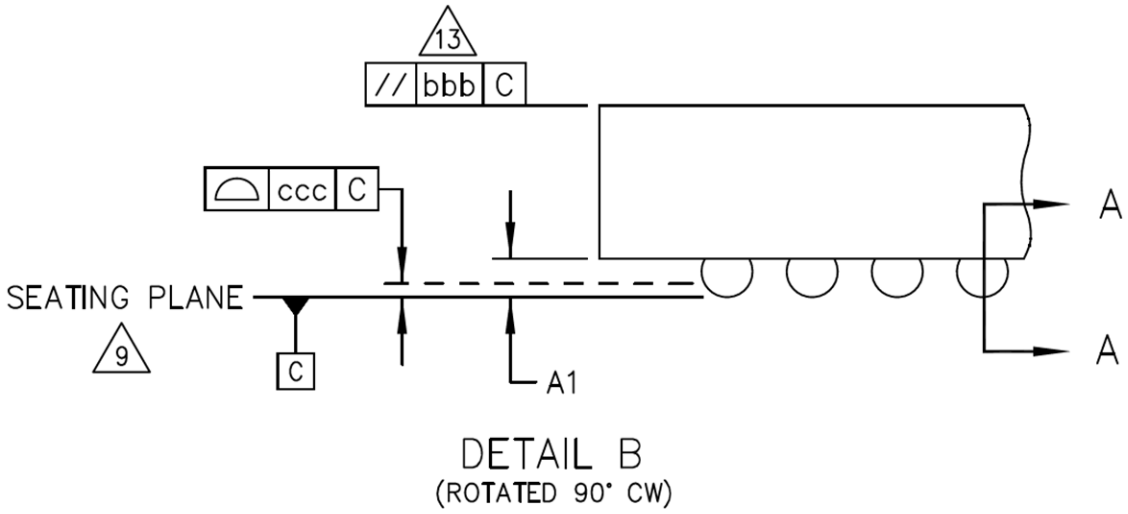
Ground 1 also teaches that the "*control circuit*" can emulate one more characteristics, e.g., in rank multiplication. *Supra* pp.8-11, 28-30; EX1003, ¶432.

12. Claim 12

Ground 1 teaches "*[t]he memory package of claim 11, wherein the chip select conduits pass through the control die.*" EX1003, ¶¶435-438. As discussed for [6.a] (pp.57-59), Ground 1 teaches "*chip select conduits*" that, as further discussed for [6.b] (pp.59-62), transmit chip-select signals up to the "*array dies*" above the "*control die*." Under the JEDEC standard, and as shown by Rajan (pp.21-30), the terminals for the chip-select signals are at the bottom of the memory package (see below), so it would be obvious for the "*chip select conduits*" to "*pass through the control die*" from the bottom to the top of the "*control die*" to transmit the chip-select signals to the "*array dies*" above the "*control die*."

EX1019, pp.6-11 ("CS" terminals at bottom of "stacked" packages); EX1021, pp.1-2 (MO-207 JEDEC standard with solder balls at the bottom of the package, below); EX1022, pp.374 ("BGA"), 476 ("FBGA"); EX1015, 6:34-38, Fig.4; EX1014, ¶¶[0028, 32], Fig.5; EX1016, ¶[0026], Fig.1; EX1003, ¶¶437-443. The 060 Patent also admits this was taught by the prior art. EX1001, 18:15-17, 19:55-56.





13. Claim 13

Ground 1 teaches "*[t]he memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array die*." EX1003, ¶¶444-449. As discussed for [6.a] (pp.57-59), Ground 1 teaches "*chip select conduits*" that, as further discussed for [6.b] (pp.59-62), transmit chip-select signals up to the "*array dies*" above the "*control die*." Drivers were well-known (pp.6-8), and it would be obvious to a POSITA that "*drivers*" would be used in the conduits of the "buffer chip" ("*control die*") of Ground 1 (*see* pp.21-30; EX1014, ¶[0032] ("chip selection command signals are buffered")) to produce enough current to transmit each chip-select signal from one chip ("*control die*") to another chip ("*array die*"). EX1030, pp.135-36 ("buffers are…used when high current flow is needed to drive external devices"); EX1038, p.68 ("tri-state drivers" are "commonly used"); EX1017, 1:14-20; EX1003, ¶447.

14. Claims 14, 16-19

The limitations of claims 14 and 16-19 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[14]	[5]	¶¶450-454 (¶¶308-313)
[16]	[1.e.4], [8.b.3][3]	¶¶472-478 (¶¶265-272, 370-376)
[17]	[1.e.4], [4.a]-[4.b]	¶¶479-483 (¶¶265-272, 291-307)
[18]	[2], [4.a]-[4.b]	¶¶484-488 (¶¶273-280, 291-307)
[19.a]	[1.e.4], [3], [4.a], [8.b.3]	¶¶490-493 (¶¶265-272, 281-289, 291-295, 370-376)
[19.b]	[1.e.4], [3]	¶¶ 494-497 (¶¶265-272, 281-289)

15. Independent Claim 29

a) ***[29.a] Memory Module***

Ground 1 teaches "*[a] memory module* [e.g. Kim's stacked memory devices implemented in Rajan's memory module (below), which can be a JEDEC-standard

[3] *See also* EX1015, 7:4-21 (describing generation of chip-select signals from "*an address signal in the control/address signals*"); pp.8-11, 21-30 (rank multiplication).

DIMM format to be used in host systems with JEDEC-standard DIMM sockets] *operable via a memory control hub* [e.g., the host system's JEDEC-compliant memory controller]." EX1015, 1:28-32 ("dual in-line memory modules (DIMMs)"), 3:5-7 ("memory controller (not shown)"), 8:52-54, 15:3-12, Fig.8 ("DIMM 800," first below); EX1014, ¶[0050]; EX1022, pp.316-20 (describing "memory controller" for JEDEC-compliant systems), Fig.7.2 (second below); EX1037, Fig.1, 1:34-39 ("Memory Controller Hub (MCH)"); EX1003, ¶¶591-598.

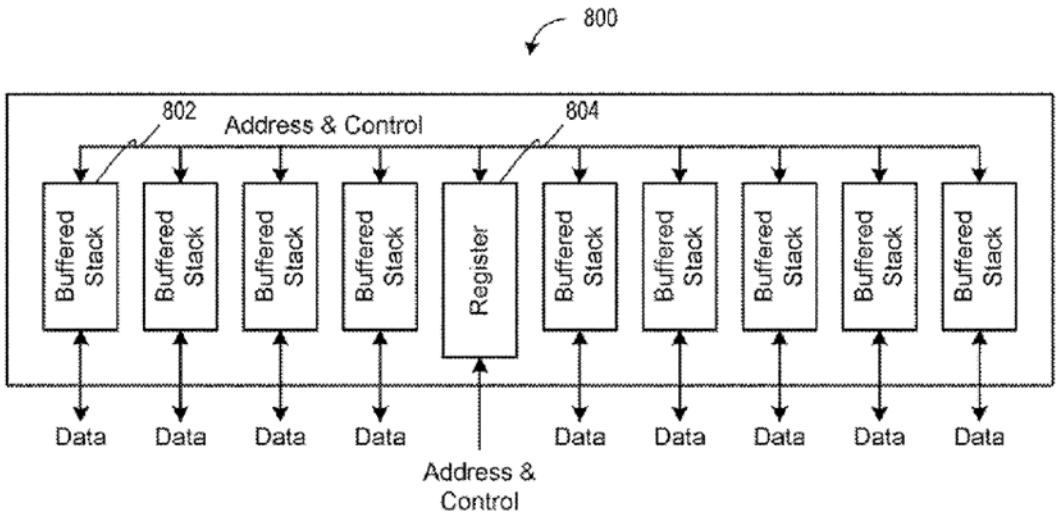


FIG. 8

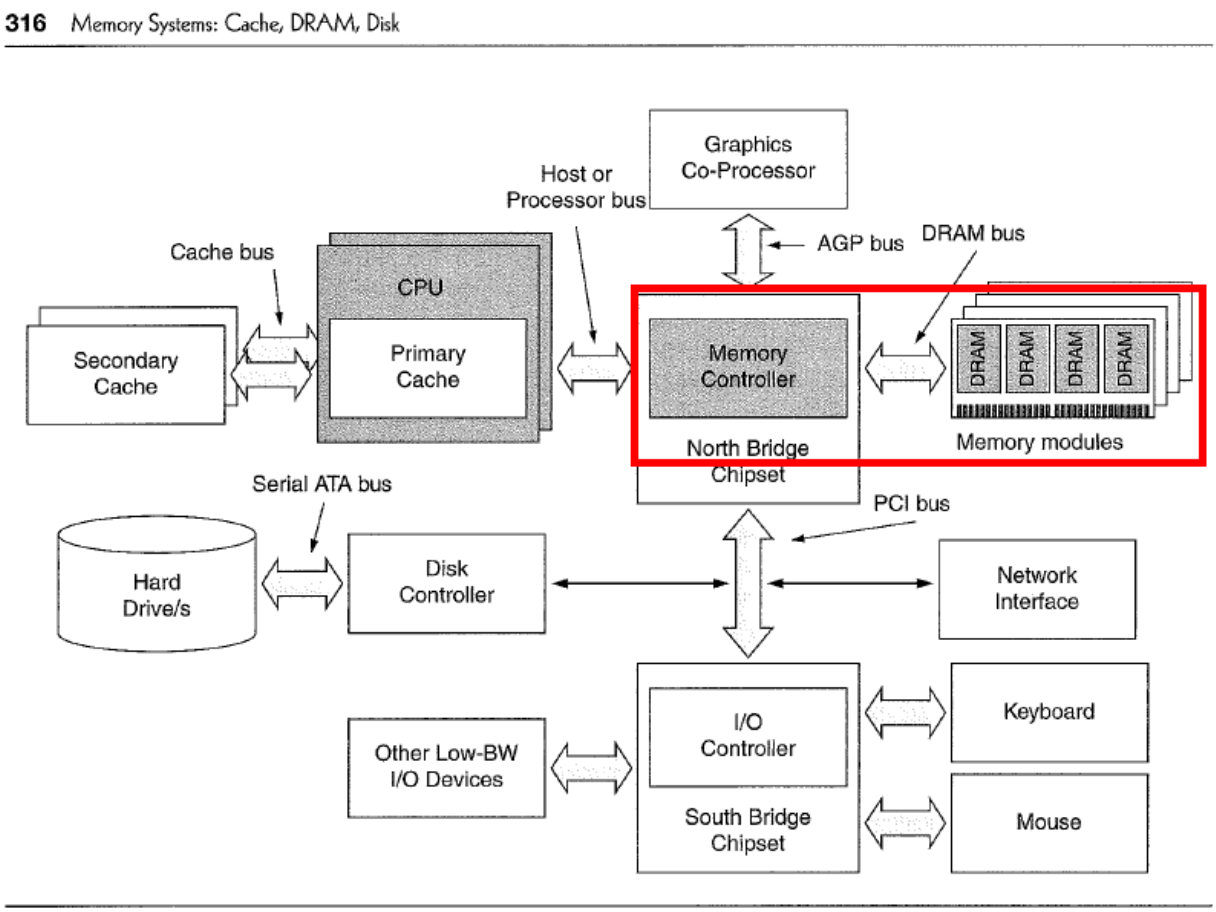


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

b) ***[29.b] Register Device***

Ground 1 teaches "*a register device* [e.g., Rajan's register 804, *see* EX1015, 8:52-58, Fig.8 (below)] *configured to receive command/address signals* [*see id.*; claim [4.a] (pp.51-53)] *from the memory control hub* [from [29.a] above] *and to generate control signals* [e.g., Rajan's register generating "Address & Control" signals (below), *see also* claim 30 (p.78)]." EX1003, ¶¶599-604, 642-649; *see also* EX1022, pp.43-44, 418-19 ("Registered Memory Module (RDIMM)").

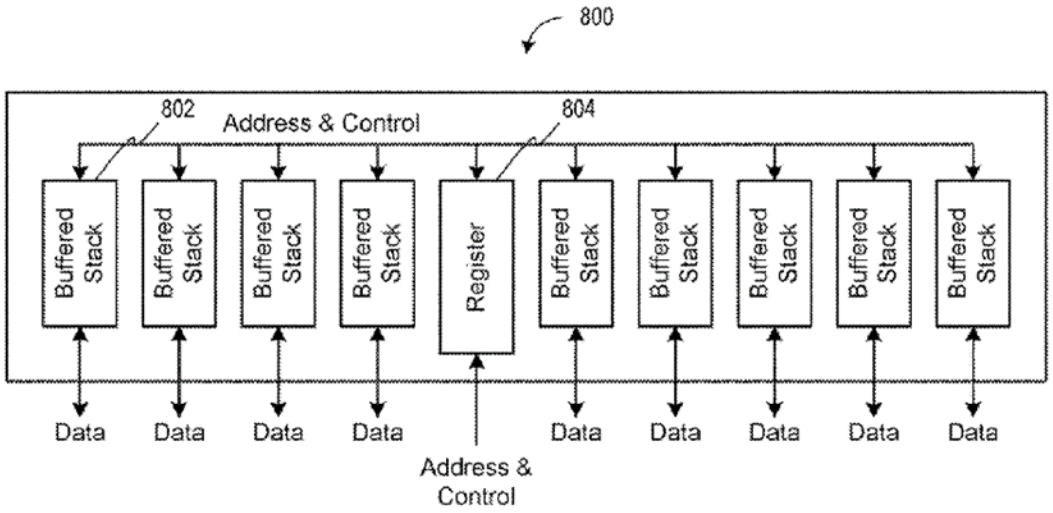


FIG. 8

c) ***[29.c]-[29.g.4]***

The limitations [29.c]-[29.g.4] are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[29.c]	[1.a][4]	¶¶605-609 (¶¶184-188)
[29.d.1]	[1.b]	¶¶610-613 (¶¶189-210)
[29.d.2]	[1.b]	¶¶614-617 (¶¶189-210)
[29.e]	[1.c]	¶¶618-621 (¶¶211-229)

[4] *See also* EX1015, Fig.8 (above), 8:52-58 (describing use of "a plurality of buffered stacks of DRAM circuits"); EX1022, pp.315, 374 (DRAM "packages").

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[29.f]	[1.d.1]-[1.d.2]	¶¶622-625 (¶¶230-239)
[29.g.1]	[1.e.1]	¶¶626-629 (¶¶240-247)
[29.g.2]	[1.e.2]-[1.e.3]	¶¶630-633 (¶¶248-264)
[29.g.3]	[4.a]-[4.b], [6.a]-[6.b][5]	¶¶634-637 (¶¶290-307, 314-334)
[29.g.4]	[11.e.5]	¶¶638-641 (¶¶425-434)

16. Claim 30

Ground 1 teaches "*[t]he memory module of claim 29, wherein the register device* [from [29.b] (pp.76-77)] *is further configured to perform rank multiplication by generating the chip select signals* [see pp.8-11 (rank multiplication); EX1015, 3:27-30, 6:30-7:67, 8:56-58 ("In one embodiment the emulation is performed at the DIMM level.")]*, and wherein the control signals include the chip select signals* [from [29.d.2] and [29.g.3] above]." EX1003, ¶¶642-649. The 060 Patent also admits this was taught by the prior art. EX1001, 18:45-51, 22:34-40, Fig.7.

[5] E.g., the array dies' received chip-select signals are buffered or generated from the control die's received chip-select signals. EX1003, ¶637; *supra* pp.8-11, 51-56, 57-62.

17. Claim 31

Ground 1 teaches "*[t]he memory module of claim 29, wherein the control signals include data path control signals* [see claim 2 (pp.47-49), e.g., chip-select signals] *generated by the register device* [see claim 30 (p.78); *see also* claim [29.b] (pp.76-77)]*, the data path control signals being used to control the respective states of the first data conduit and the second data conduit* [see claim [1.e.4] (pp.46-47) and claim 2 (pp.47-49); *see also* claim [29.g.4] (p.78)]." EX1003, ¶¶650-658.

18. Claim 32

Ground 1 teaches "*[t]he memory module of claim 29, wherein the control die* [from [29.g.1] (p.78)] *is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal* [see pp.8-11, 21-30 (rank multiplication); claim 16 (p.74); EX1015, 3:27-30, 6:30-7:67, Fig.18]." EX1003, ¶¶659-668.

19. Claim 33

Ground 1 teaches "*[t]he memory module of claim 29, wherein the control signals include command/address signals* [see claim [4.a] (pp.51-53)]*, and the control die is configured to hold the command/address signals to control timing of the command/address signals* [e.g., Rajan's buffer chip receives command/address signals for a write command and holds those signals for "an extra two clocks of delay" to control the timing of when the stacked DRAMs receive those signals,

EX1015, 9:46-10:27, Fig.11 (below)]." EX1003, ¶¶669-676. A POSITA would have been motivated by Rajan's teachings to implement this command/address signal delay in Kim's device to emulate the characteristics of JEDEC-standard memory devices, including timing. EX1015, 9:46-10:4; EX1019, pp.23-24 ("CAS latency"); EX1003, ¶674.

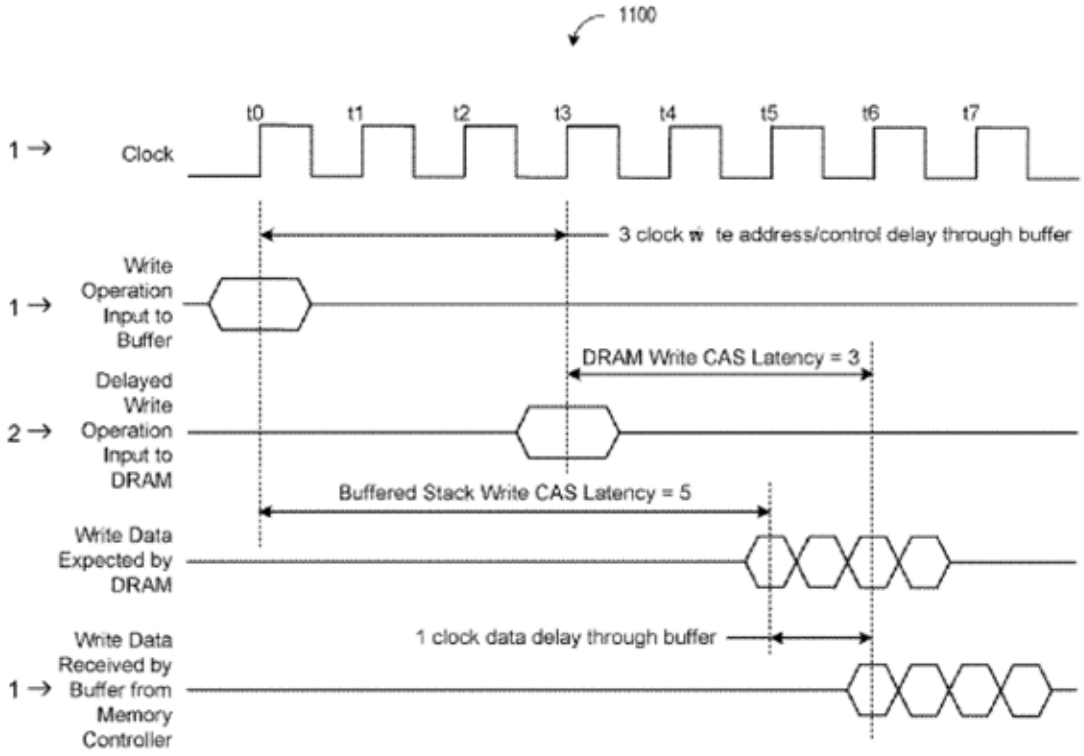


FIG. 11

20. Claim 34

Ground 1 teaches "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective*

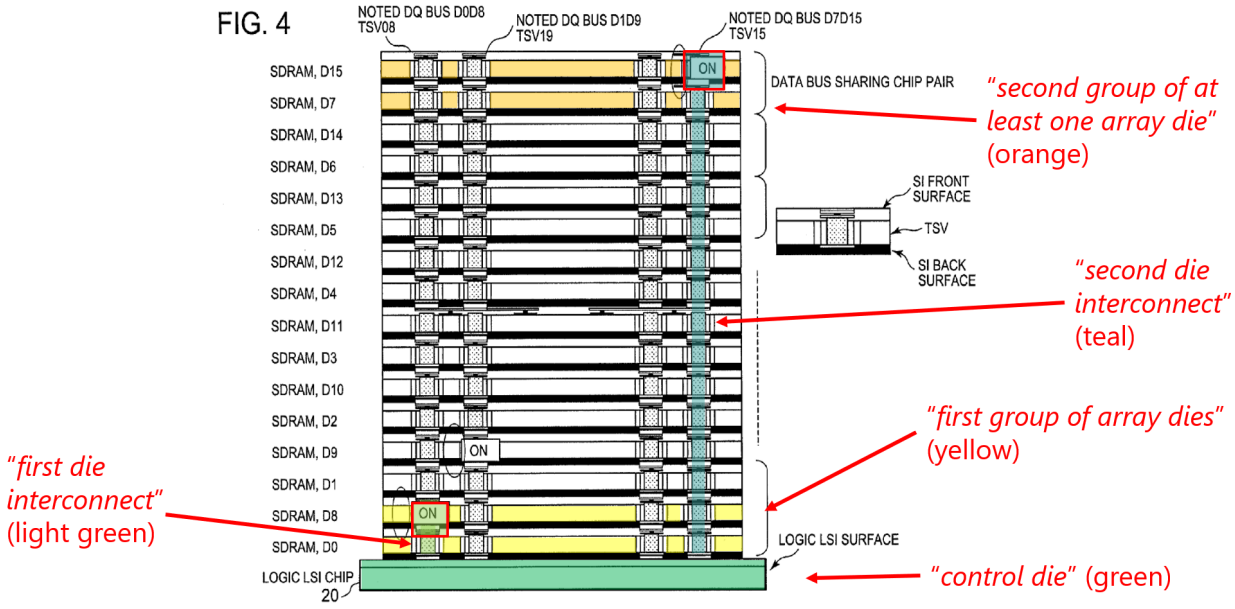
states of the first data conduit and the second data conduit," as explained for claim element [1.e.4] (pp.46-47) and claim 3 (pp.49-51). EX1003, ¶¶677-681.

B. Ground 2 (Ground 1 + claim 7)

1. Ground 2 combination: Ground 1 and Riho (EX1016)

Ground 2 is based on Ground 1 (Kim in view of Rajan) in further view of Riho (EX1016). EX1003, ¶¶169-173. Ground 2 thus renders obvious the same claims as Ground 1, plus claim 7 as discussed below.

As explained above (pp.21-30), a POSITA would have been motivated to look at analogous art, and Riho is analogous since it is also directed to the operation of stacked memory devices and discloses the same basic structure (below), including stacked memory chips (yellow, orange) and a shared interface circuit (green), called the "logic LSI chip" in Riho. EX1016, ¶¶[0002, 0062], Fig.4 (below); EX1003, ¶171.



Riho teaches using ***pairs*** of SDRAM memory chips, where each pair shares a TSV for data signals (DQ), such as pair D0/D8 (yellow) coupled to DQ bus D0D8 including TSV08, and pair D7/D15 (orange) coupled to DQ bus D7D15 including TSV15, with only ***one*** of the two SDRAMs in the pair connected to the TSV at a time, thus "reduc[ing] by half the load." EX1016, ¶¶[0062, 0103]; EX1003, ¶172.

Kim teaches that "any number" of chips may be stacked, EX1014, ¶¶[0048, 0050], and thus a POSITA would have been motivated with a reasonable expectation of success (when adding chips to Kim) to use Riho's technique described above to further reduce the load (allowing for higher-frequency operations) and to compensate for phase variations, as taught by Riho, without the need to create additional TSVs. EX1003, ¶¶172-173; EX1016, ¶¶[0119-20].

2. Claim 7

a) ***[7.a] First and Second Number of Array Dies***

Ground 2 teaches "*[t]he memory package of claim 1, wherein a first number of* [two] *array dies in the first group of array dies* [sharing a data signal TSV] *and a second number of at least one array die* [two dies] *in the second group of at least one array die* [sharing another data signal TSV] *are selected in consideration of a load of the first die interconnect and a load of the second die interconnect* [including the load of each of those data signal TSVs] *so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit* [so the "skew between data signals DQ and data strobe signals DQS/B can be minimized" allowing a "single synchronization signal with high accuracy," EX1016, ¶¶[0050, 0053-54]]." EX1003, ¶¶336-343; *see also supra* pp.6-8 (more load creates more delay); EX1019, p.13 ("Data Strobe" for reads and writes).

b) ***[7.b] First and Second Load***

Ground 2 teaches "*the first load including a load of the first die interconnect* [on one data signal TSV], *and a load of the first group of array dies* [including a pair of SDRAM chips], *and the second load including a load of the second die interconnect* [on another data signal TSV] *and a load of the second group of at least one array die* [including another pair of SDRAM chips]." EX1016, ¶¶[0013, 0132] ("load of the interconnections" and "load…from the…SDRAM"); EX1003, ¶¶344-350; *see also supra* pp.6-8 (load was well known).

C. Ground 3 (Ground 1 + claims 15, 20-28)

1. Ground 3 combination: Ground 1 and Wyman (EX1017)

Ground 3 is based on Ground 1 (Kim in view of Rajan) in further view of Wyman (EX1017). EX1003, ¶¶174-181. Ground 3 thus renders obvious the same claims as Ground 1, plus claims 15 and 20-28 as discussed below.

Wyman is analogous art to Kim and the 060 Patent: its goal is to improve efficiency of signaling between stacked chips. EX1017, 1:45-48; EX1001, 1:19-21, 5:23-26; EX1014, ¶¶[0003, 0046]; EX1003, ¶¶178, 180. Wyman discloses that shorter paths (e.g., 802 below) have less load and thus require less drive, while longer paths (e.g., 804 below) have more load and thus require a larger drive, but it would be "wasteful" and "overkill" to use the "full capacity" of a driver for either path. EX1017, 1:22-24, 1:45-48, 6:15-50, 7:13-18, Fig.8 (below); *see also supra* pp.6-8 and EX1030, pp.135-138 (disclosing different-sized transistors to achieve different driver strengths).

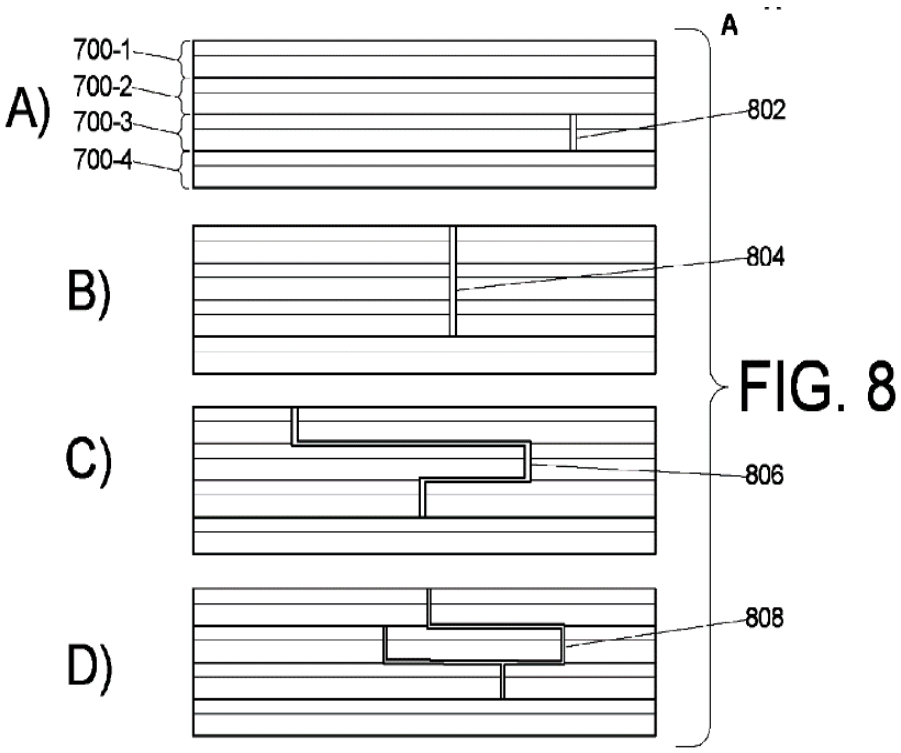
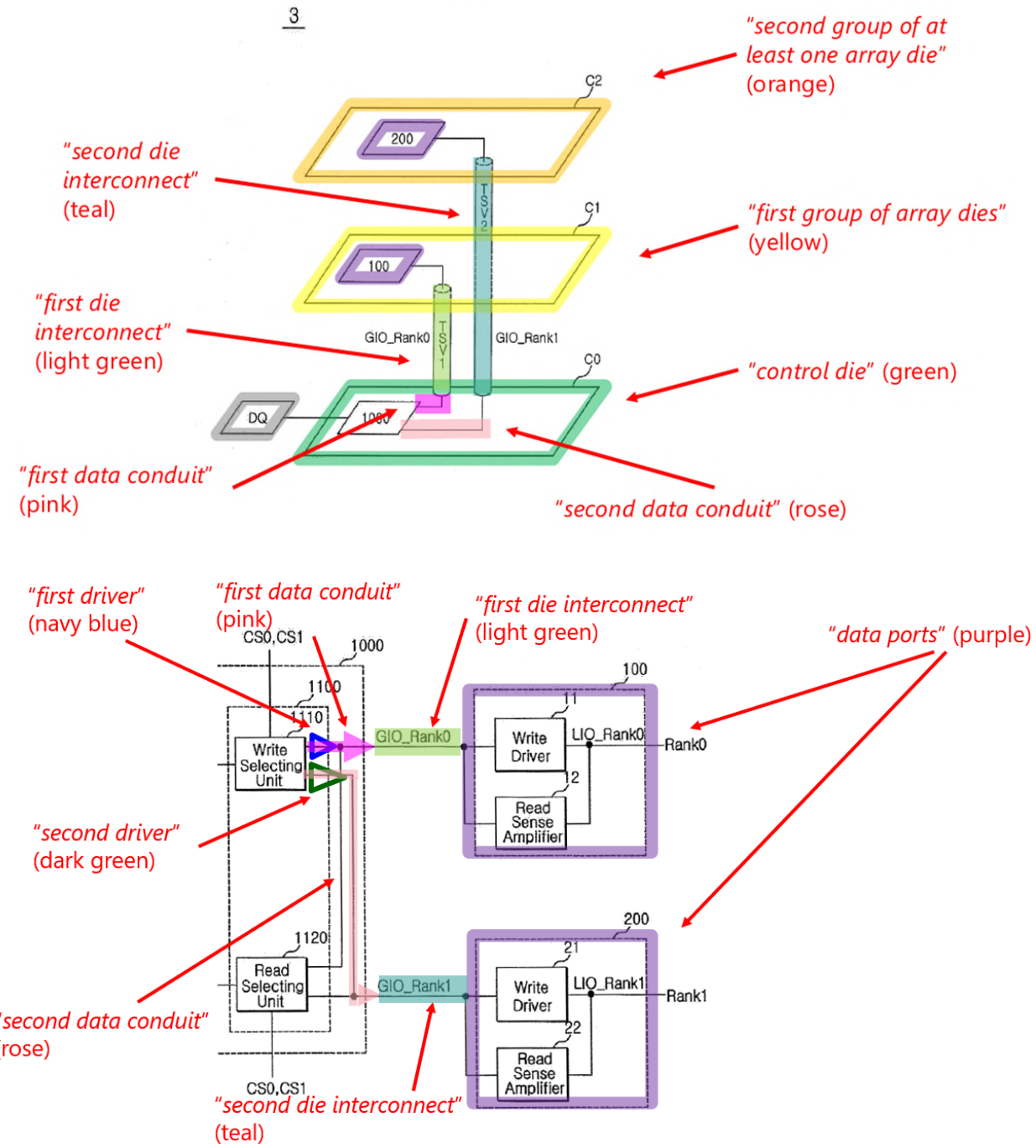


FIG. 8

A POSITA would have been motivated to implement Wyman's teachings in Kim to improve power efficiency by using a smaller driver (navy blue) for the shorter TSV1 (light green) and a larger driver (dark green) for the longer TSV2 (teal), as shown below, without using the full strength of a driver which Wyman teaches would be "wasteful and inefficient." *Id.*; EX1003, ¶¶177-180.

FIG.5

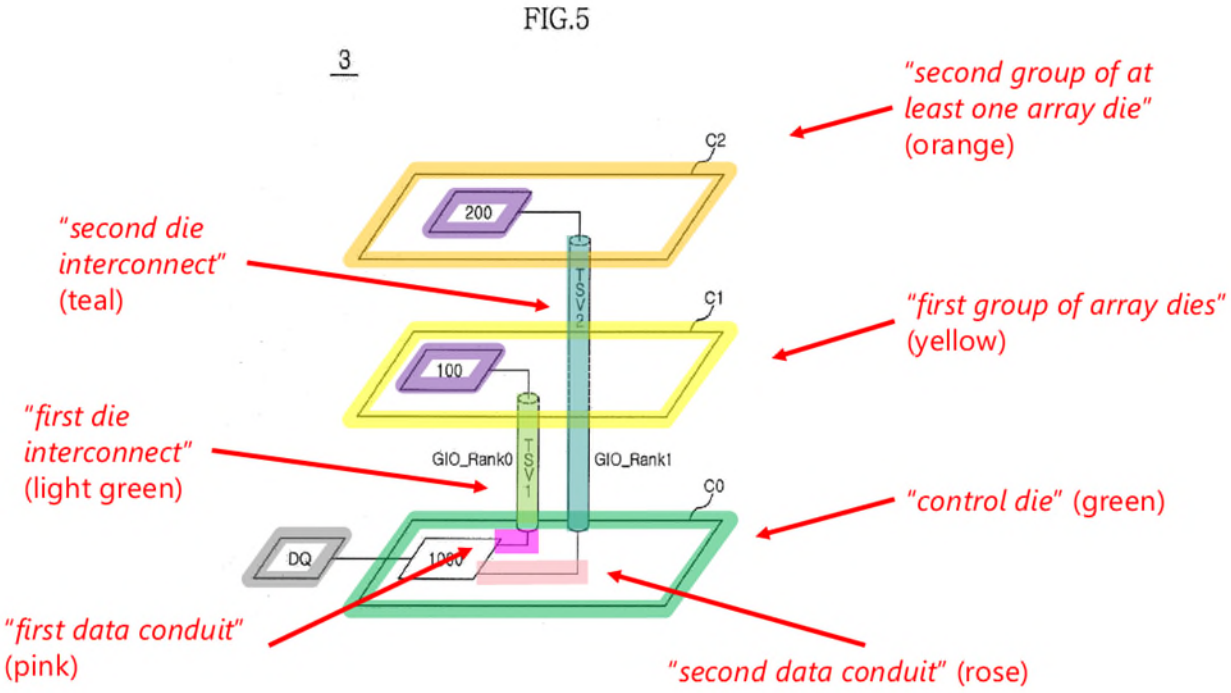

3
"second group of at least one array die" (orange)
C2
200
"second die interconnect" (teal)
TSV2
C1
"first group of array dies" (yellow)
100
"first die interconnect" (light green)
GIO_Rank0
TSV1
GIO_Rank1
C0
"control die" (green)
DQ
1000
"first data conduit" (pink)
"second data conduit" (rose)
"first driver" (navy blue)
"first data conduit" (pink)
CS0,CS1
1000
"first die interconnect" (light green)
"data ports" (purple)
1100
100
1110
11
Write Selecting Unit
GIO_Rank0
Write Driver
LIO_Rank0
Rank0
12
Read Sense Amplifier
"second driver" (dark green)
200
1120
21
Read Selecting Unit
GIO_Rank1
Write Driver
LIO_Rank1
Rank1
22
Read Sense Amplifier
"second data conduit" (rose)
CS0,CS1
"second die interconnect" (teal)

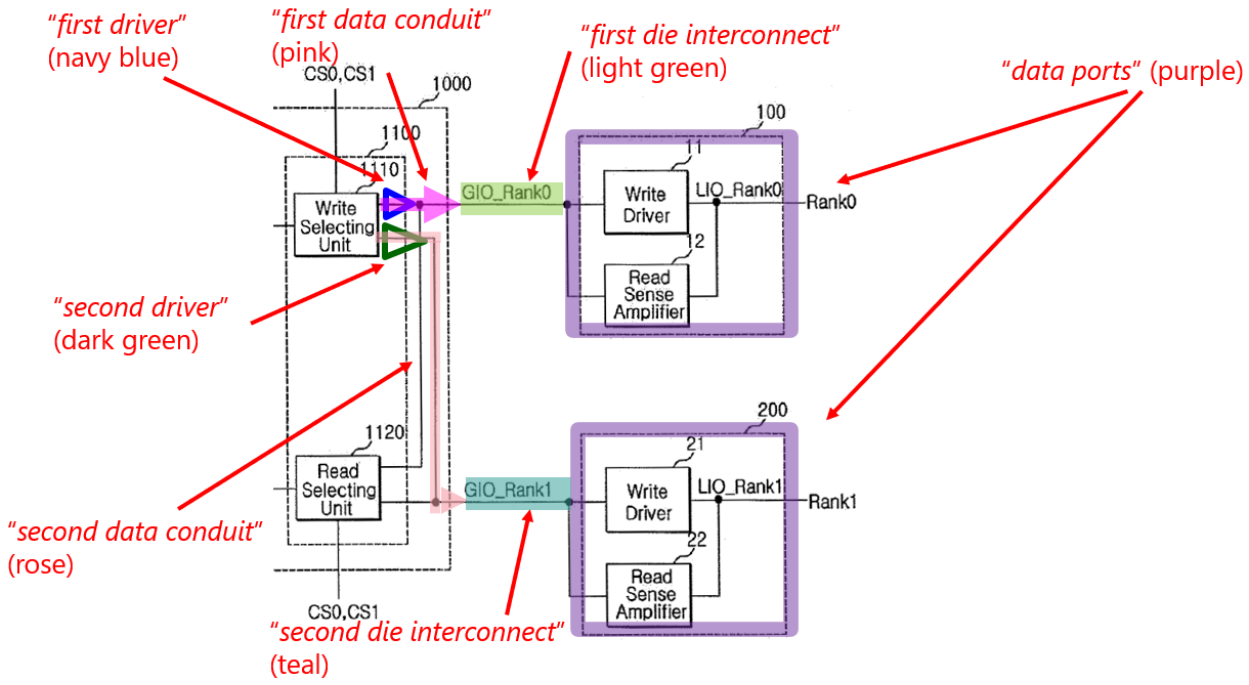
2. Claim 15

a) *[15.a] First and Second Data Conduit*

Ground 3 teaches "*[t]he memory package of claim 11, wherein: the first data conduit* [(pink) to TSV1, *see* claim [1.e.2] (pp.42-45)] *comprises at least a first driver having a first driver size* [smaller navy blue triangle, below]*, and the second data conduit* [(rose) to TSV2, *see* claim [1.e.3] (pp.42-45)] *comprises at least a second driver having a second driver size* [larger dark green triangle, below]*, and*." EX1014, Figs. 3, 5 (below); EX1003, ¶¶456-464.

FIG.5





Given that Kim expressly illustrates in Figure 5 above that TSV1 is shorter than TSV2, a POSITA would have understood from Wyman the benefit of using a different driver size for each data conduit that is optimized for efficiently driving data signals through corresponding TSVs to avoid "wasteful and inefficient" use of power, as explained more fully above (pp.84-86). EX1003, ¶¶456-464.

b) ***[15.b] Driver Size***

Ground 3 teaches "*wherein the first driver size* [smaller navy blue triangle, above] *and the second driver size* [larger dark green triangle, above] *are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies* [from [11.c] (p.69)] *without significant signal degradation*." EX1003, ¶¶465-471. As shown above, Kim's TSV1 and TSV2 are each coupled to circuitry in some, but not all, of the slave

chips in the stack, requiring less driver strength than if ***all*** the slave chips were connected, and Wyman teaches to choose a driver size that will "adequately drive" the signal but is still less than the "total drive," which would be "overkill" and inefficient. *Id.*; EX1017, 1:45-47, 6:57-60; *supra* pp.84-86.

3. Claims 20-28

The limitations of claims 20-28 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 3 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[20.a]	[1.a][6]	¶¶499-502 (¶¶184-188)
[20.b.1]	[1.c]	¶¶503-506 (¶¶211-229)
[20.b.2]	[1.d.1]-[1.d.2]	¶¶507-510 (¶¶230-239)
[20.b.3]	[1.e.1]	¶¶511-514 (¶¶240-247)
[20.b.4]	[1.b]	¶¶515-518 (¶¶189-210)
[20.c]	[20.a]	¶¶519-522 (¶¶499-502)
[20.d.1]	[1.b], [1.e.2]-[1.e.3]	¶¶523-526 (¶¶189-210, 248-264)
[20.d.2]	[1.b], [1.e.4]	¶¶527-530 (¶¶189-210, 265-272)

[6] The specific steps for "*optimizing [the] load*" are explained in the subsequent limitations.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[20.d.3]	[4.a]-[4.b], [6.a]-[6.b][7]	¶¶531-534 (¶¶291-307, 315-334)
[20.d.4]	[11.e.5], [15.a]	¶¶535-538 (¶¶425-434, 456-464)
[20.e.1]-[20.e.2]	[1.d.1]-[1.d.2]	¶¶539-542 (¶¶230-239)
[21]	[15.a]-[15.b][8]	¶¶543-547 (¶¶456-471)
[22]	[15.b]	¶¶548-552 (¶¶465-471)
[23]	[16]	¶¶553-557 (¶¶472-478)
[24]	[4.a]-[4.b][9]	¶¶558-562 (¶¶291-307)
[25]	[5]	¶¶563-567 (¶¶308-313)

[7] See note 5 on p.78.

[8] The combination of Kim and Wyman teaches that the driver size is selected based on the load (including the length of the TSV). *See supra* pp.84-86; EX1003, ¶547.

[9] Under the JEDEC standard, the signals indicating the "*command*" include "CS#," i.e., the "*chip-select signal*." EX1019, pp.13, 33; EX1003, ¶562; *supra* pp.31-34.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[26]	[12][10]	¶¶568-575 (¶¶435-443)
[27.a]	[3]	¶¶577-580 (¶¶281-289)
[27.b]	[3], [11.e.5], [15.a]	¶¶581-584 (¶¶281-289, 425-434, 456-464)
[28]	[3], [11.e.5], [15.a]	¶¶585-589 (¶¶281-289, 425-434, 456-464)

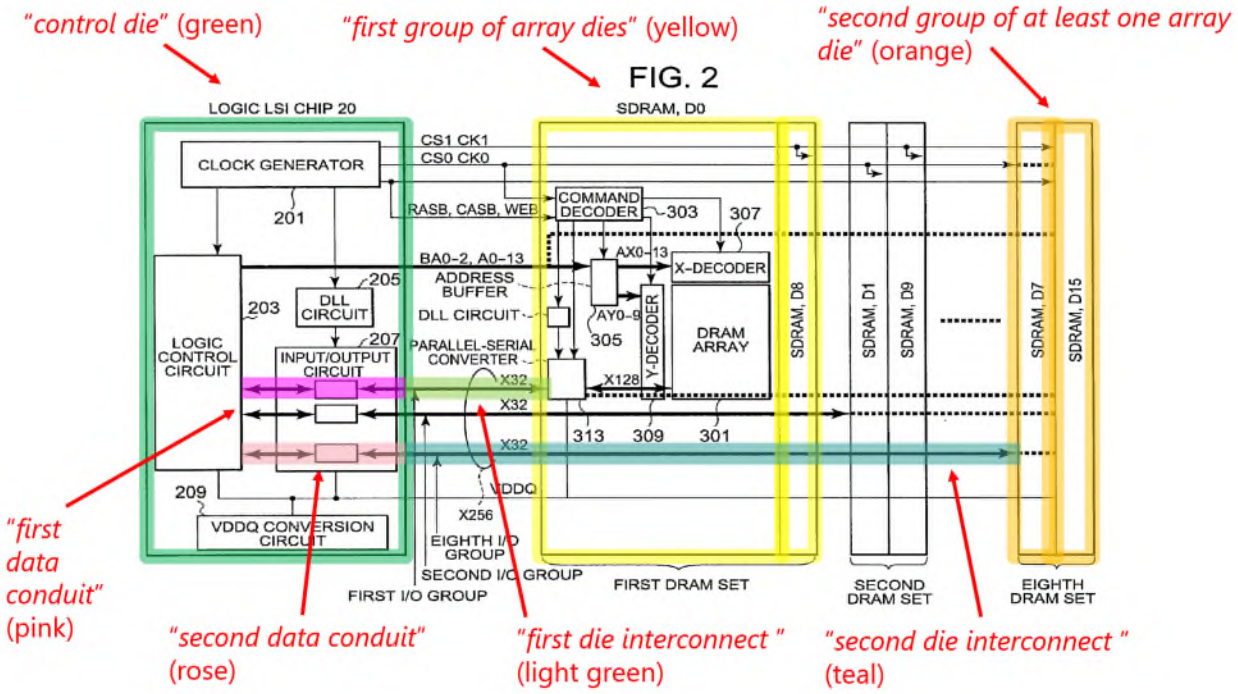
D. Ground 4 (claims 1-14, 16-19, 29-34)

1. Ground 4 combination: Riho (EX1016) and Rajan (EX1015)

Ground 4 combines Riho (EX1016) with Rajan (EX1015), both of which, like the 060 Patent, disclose the same basic memory package structure including groups of stacked memory chips (yellow, orange) and a shared interface circuit (green). EX1016, ¶¶[0002, 12], Fig.2 (first below); EX1015, 1:51-60, 2:6-7, 4:48-50, Fig.4 (second below); EX1001, 1:18-21, 5:23-26, Fig.2 (above p.14); EX1003, ¶¶683-692.

[10] Furthermore, it was well-known at the time to use TSVs for passing signals through a die, as admitted by the 060 Patent. EX1001, 1:49-2:7, Figs.1A-1B (describing prior art); EX1014, ¶[0046]; EX1016, ¶[0030], Fig.1; EX1003, ¶573.

Riho:



Rajan:

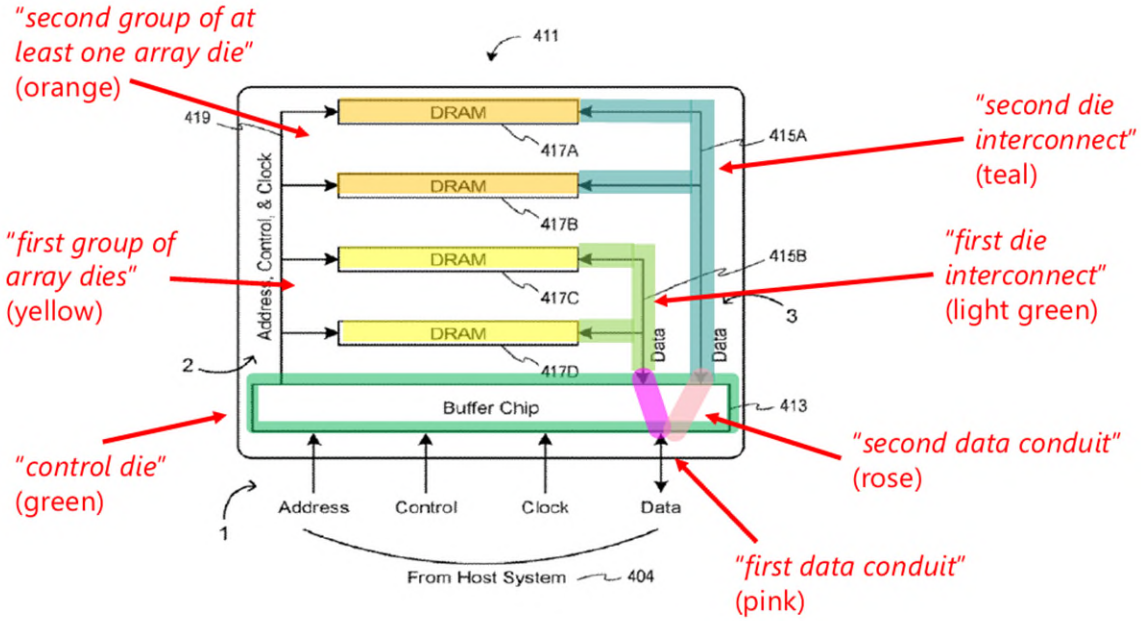


FIG. 4

A POSITA would have been motivated to combine Riho and Rajan for at least two reasons. First, as explained and shown above, they are analogous art with similar structures, so a POSITA would be motivated to look at the details taught by Rajan when implementing Riho, including details about the interface chip (green) and the external terminals to the host, which are "not illustrated" in Riho. EX1003, ¶¶685-689; EX1016, ¶¶[0026, 0030].

Second, a POSITA would be motivated to create a package with an interface that complied with the well-known JEDEC standards, as taught by Rajan. EX1003, ¶¶689-691. Specifically, a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system — including the use of "rank multiplication" (discussed above, pp.8-11) — and to follow Rajan's suggestion to implement address, control and data terminals according to JEDEC standards (including the DDR3 standard for stacked memory devices shown below, EX1019, p.12, Fig.3, and the GDDR4 standard, EX1035, p.2). *Id.*; EX1015, 2:6-7, 3:52-54, 4:20-24, 5:36-43, 6:30-7:67, 8:8-11, Figs.4 (above), 18 (for emulation). Indeed, the JEDEC standards were influential and well-known, as discussed above (p.6).

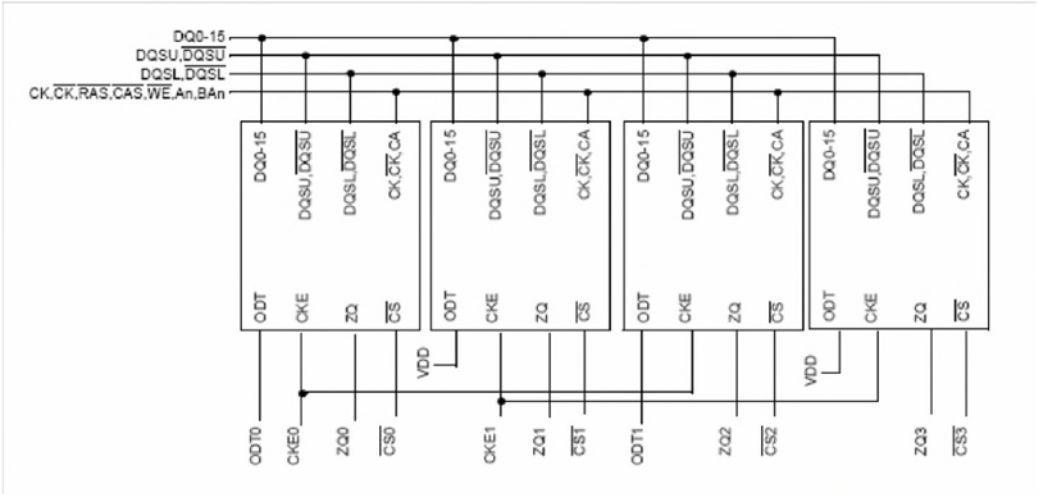


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

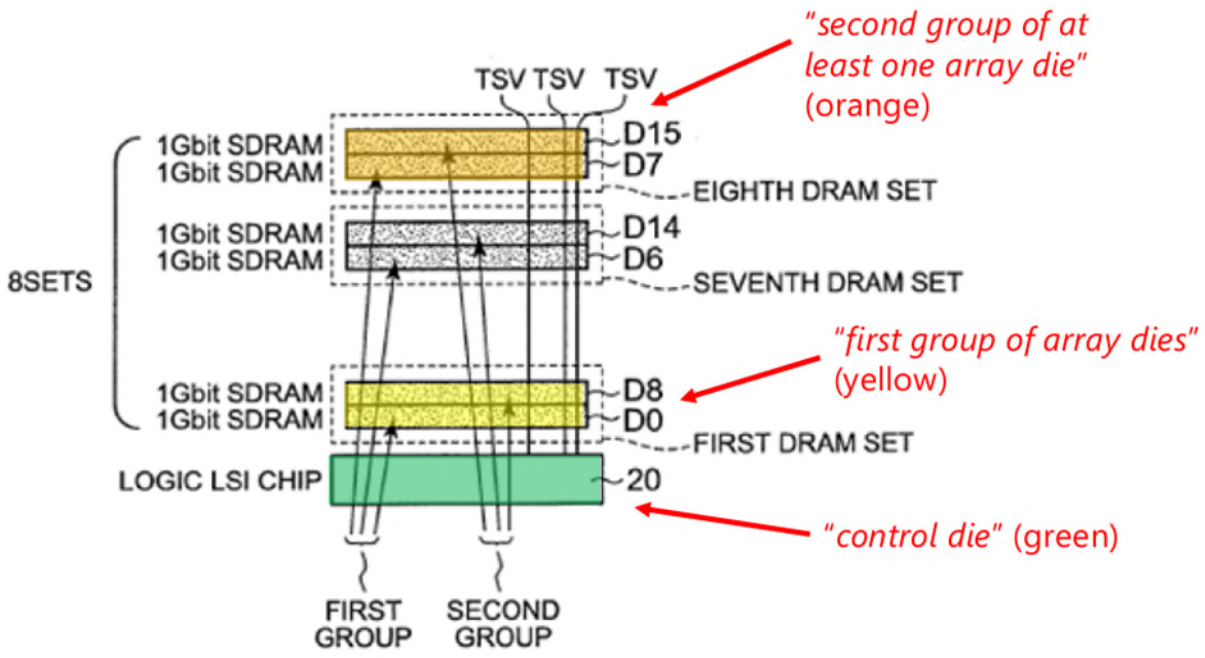
Such a combination would have been well within a POSITA's level of skill since emulating a standard JEDEC interface was well-known, as demonstrated by Rajan (discussed directly above) and the 060 Patent's admitted prior art (discussed above, pp.8-11). EX1003, ¶691; EX1001, 22:37-39.

2. Independent Claim 1

a) *[1.a] Preamble*

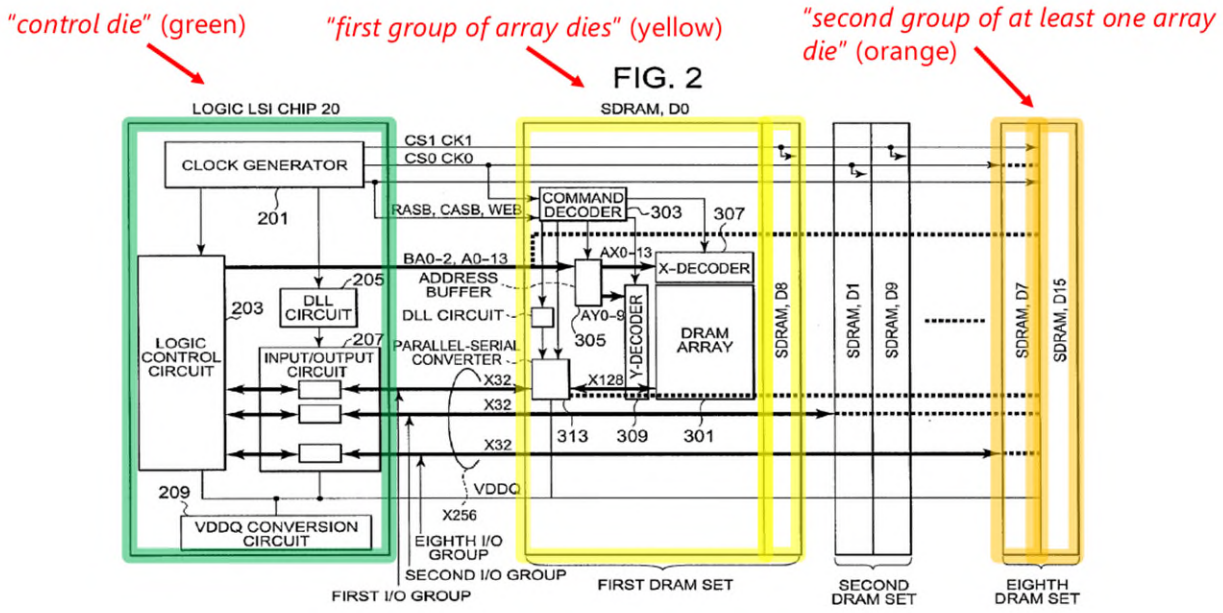
To the extent the preamble is limiting, Ground 4 teaches "*[a] memory package* [e.g., Riho's "packaged" "semiconductor device" in Figure 1 (below) including a control chip (logic LSI chip 20, green) and stacked SDRAM chips (D0-D15, yellow and orange)]*, comprising*." EX1016, ¶[0026], Fig.1 (below); EX1003, ¶¶706-710.

FIG. 1



b) ***[1.b] Input/Output Terminals***

Ground 4 teaches "*a plurality of input/output terminals* [Riho's "external terminals (not illustrated)" on the "lower side" of logic LSI chip 20, green] *via which the memory package communicates data* [e.g., DQ signals along with related data mask, DM, and data strobe, DQS/DQSB, signals)] *and control* [e.g., RASB, CASB, WEB, CS0CK0, CS1CK1,…] */address* [e.g., BA0-BA2 and A0-A13] *signals with one or more external devices*." EX1016, ¶¶[0026, 0030-31], Fig.2 (below); EX1003, ¶¶711-718; *see also* EX1019, pp.6-14, 18, 33 (JEDEC standard).



Moreover, it would have been obvious to a POSITA to implement Riho's memory package with Rajan's terminals (below) to comply with the JEDEC standards, as explained above for the combination of Ground 4 (pp.91-94). EX1003, ¶¶683-692, 715-716; EX1015, Figs.4, 18 (below, illustrating a buffer chip receiving data and control/address signals from an external host system, and controlling DRAM devices in a stack).

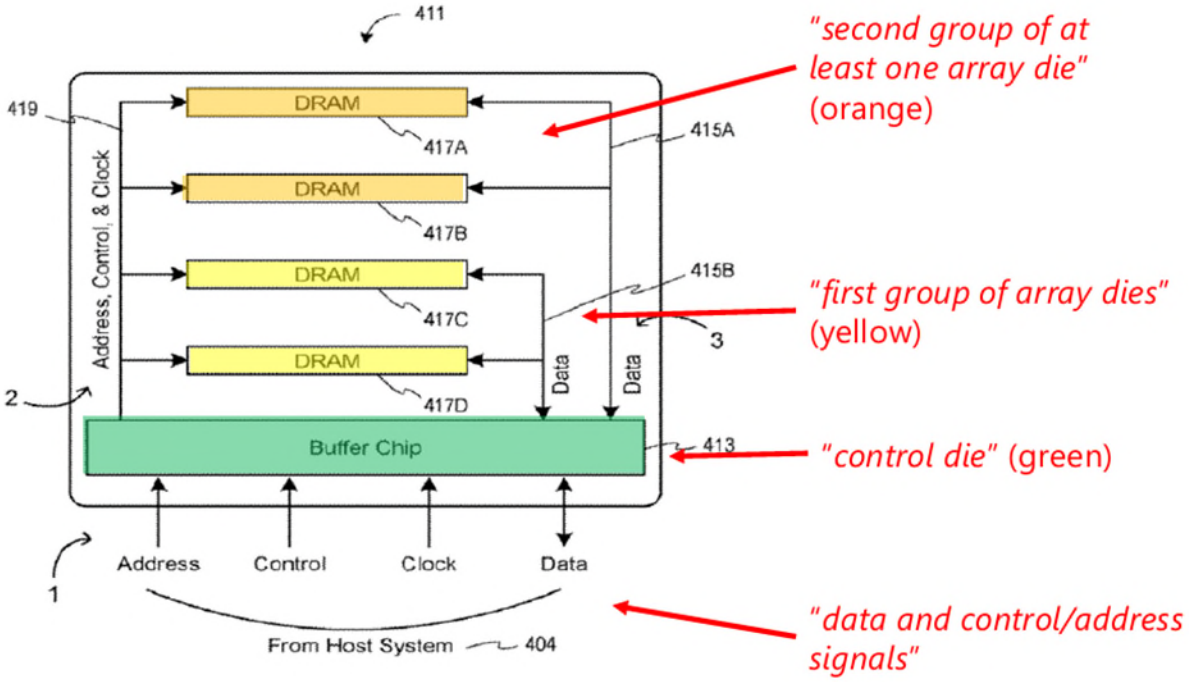

411
419
DRAM
417A
DRAM
417B
DRAM
417C
DRAM
417D
Address, Control, & Clock
415A
415B
3
Data
Data
2
Buffer Chip
413
1
Address
Control
Clock
Data
From Host System
404
"second group of at least one array die" (orange)
"first group of array dies" (yellow)
"control die" (green)
"data and control/address signals"

FIG. 4

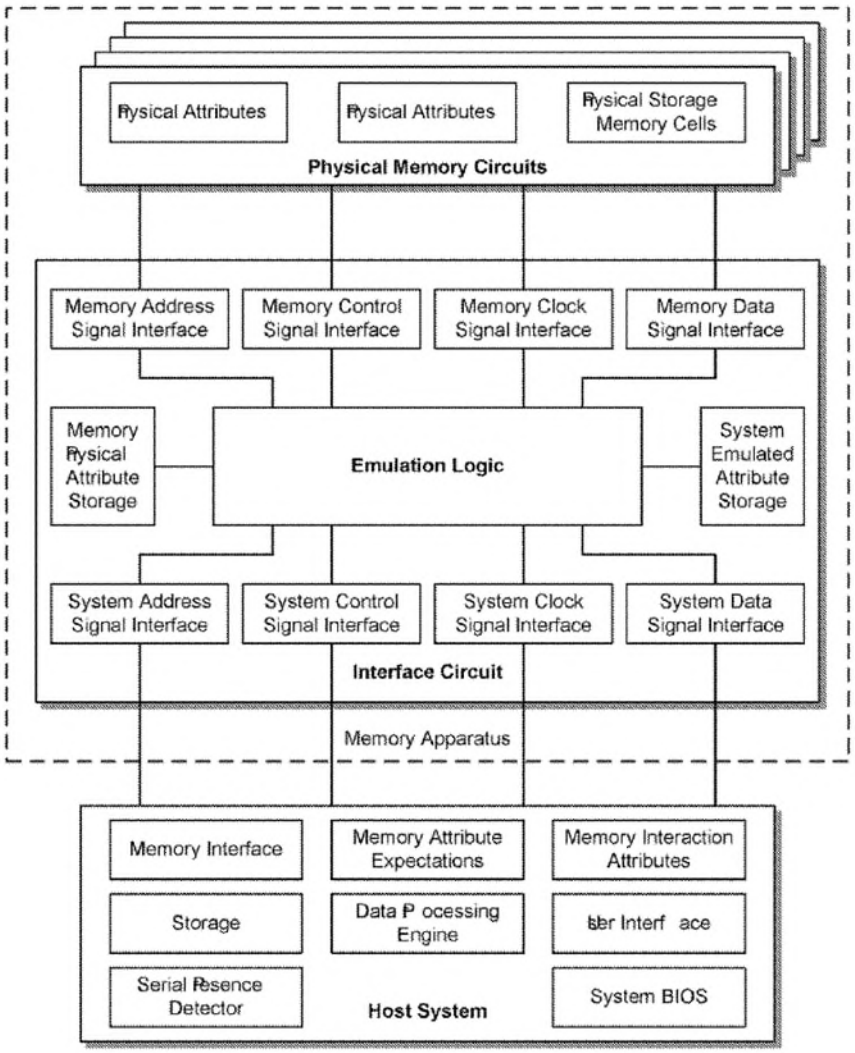


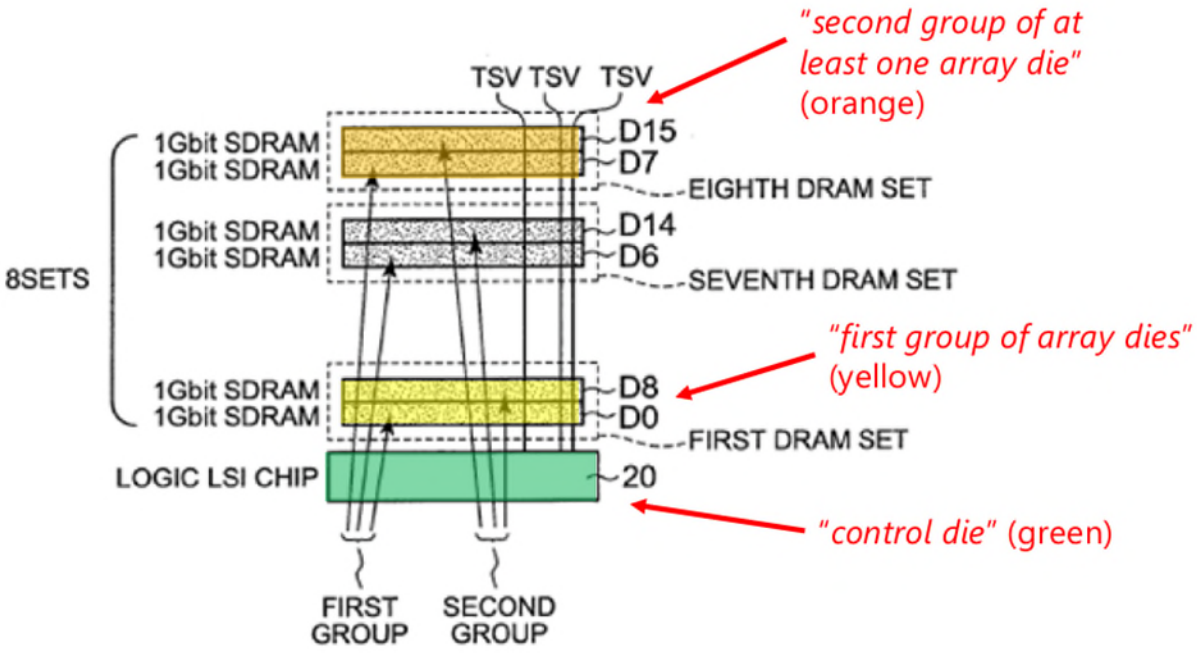
FIG. 18

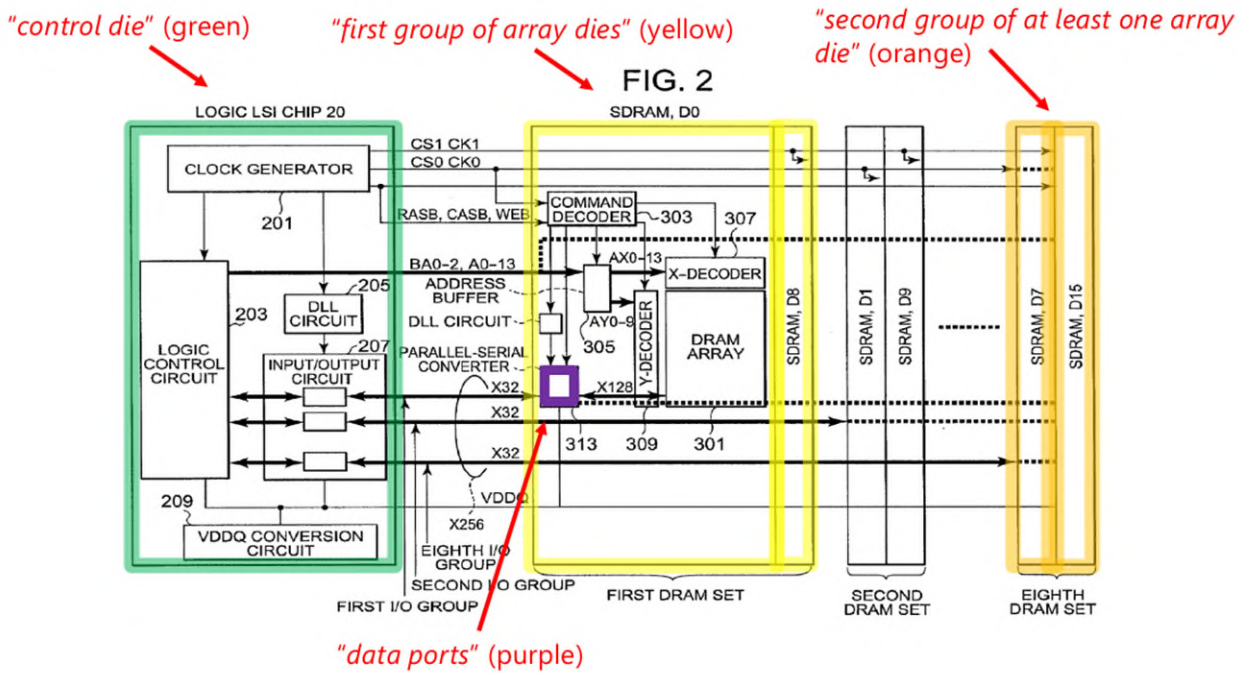
c) ***[1.c] Stacked Array Dies***

Ground 4 teaches "*a plurality of stacked array dies* [e.g., SDRAM chips D0-D15, each chip including a respective DRAM array 301] *including a first group of array dies* [e.g., a first DRAM set including the pair of SDRAMs D0 and D8 sharing data signal DQ TSV08 (yellow)] *and a second group of at least one array die* [e.g., an eighth DRAM set including the pair of SDRAMs D7 and D15 sharing data signal DQ TSV715 (orange)]*, each array die having data ports* [including a

parallel-serial conversion circuit 313 (purple) in each SDRAM]." EX1016, ¶¶[0027, 0029, 0045-47, 0049, 0062], Figs.1-2 (below); EX1003, ¶¶719-726. A POSITA would understand that Riho's SDRAM chip includes a "die." EX1018, Abstract, Fig.1 ("stacked" "chip die[s]"); EX1003, ¶723.

FIG. 1

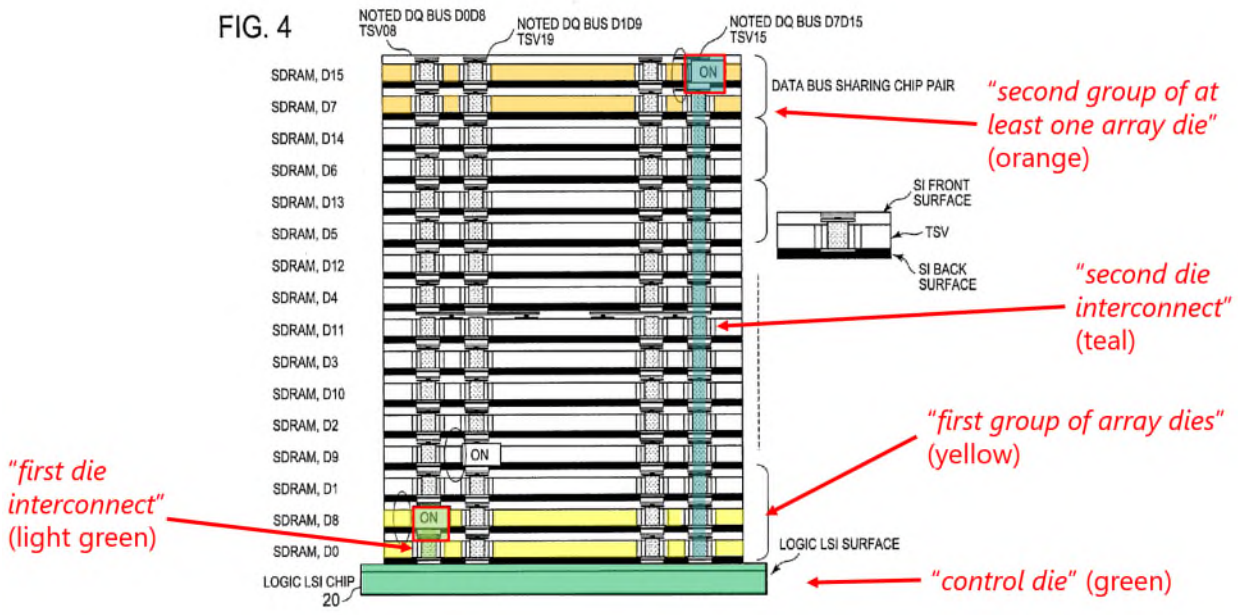


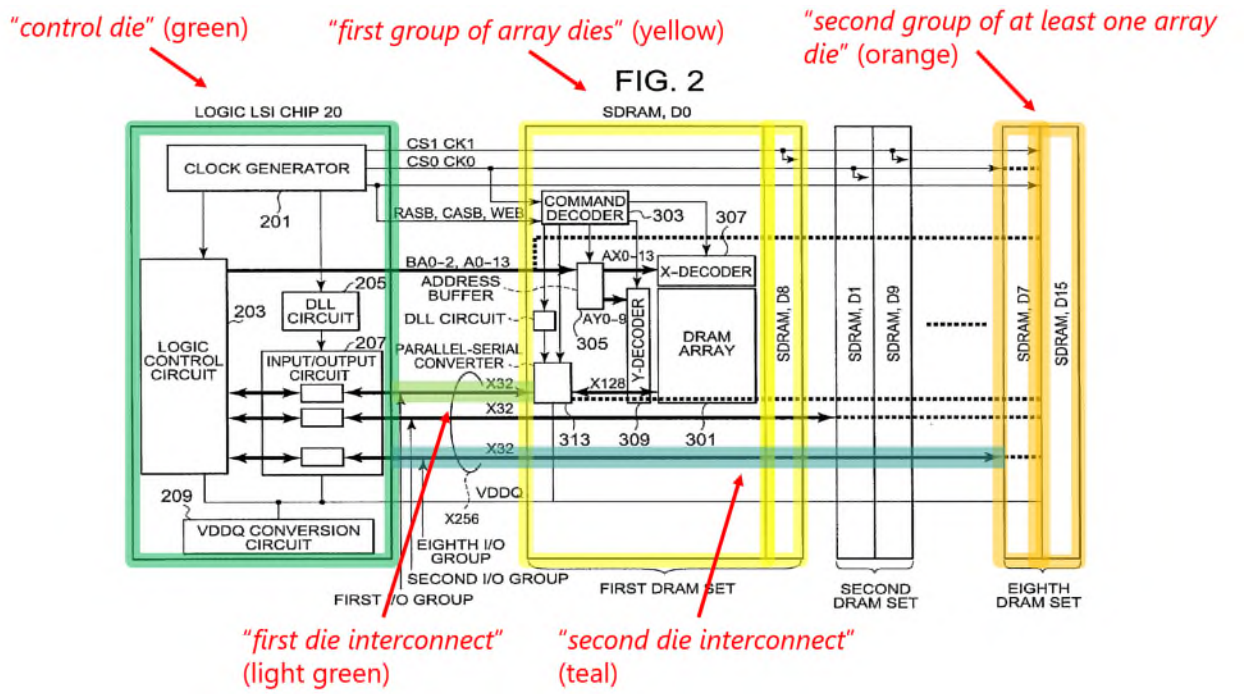


d) ***[1.d.1] and [1.d.2] Die Interconnects in Electrical Communication with Array Dies***

Ground 4 teaches "*at least a first die interconnect* [e.g., data signal DQ TSV08 (light green)] *and a second die interconnect* [e.g., data signal DQ TSV715 (teal)]*, the first die interconnect* [TSV08] *in electrical communication with the first group of array dies* [e.g., the first DRAM set including SDRAMs D0 and D8 (yellow) are in a "conductive" (i.e., "on") state] *and not in electrical communication with the second group of at least one array die* [e.g., all other SDRAMs, including the eighth DRAM set of SDRAMs D7 and D15 (orange), are in a "non-conductive" (i.e., "off") state]," and "*the second die interconnect* [TSV715] *in electrical communication with the second group of at least one array die* [including SDRAMs D7 and D15] *and not in electrical communication with*

the first group of array dies [including SDRAMs D0 and D8]*; and*." EX1016, ¶¶[0045-46, 0064-65], Figs.2, 4 (both below); EX1003, ¶¶727-744. Rajan also teaches this arrangement to reduce load (third below), further rendering obvious [1.d.1]-[1.d.2]. EX1015, 5:36-43, 5:63-6:2, Fig.4 (third below); EX1003, ¶¶739-743.





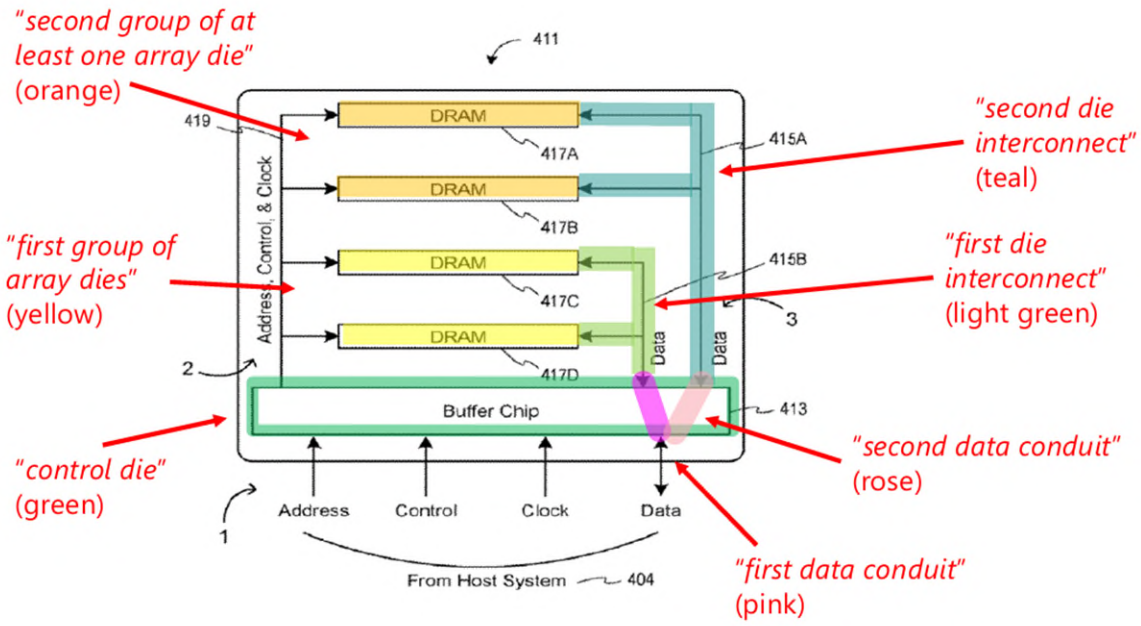


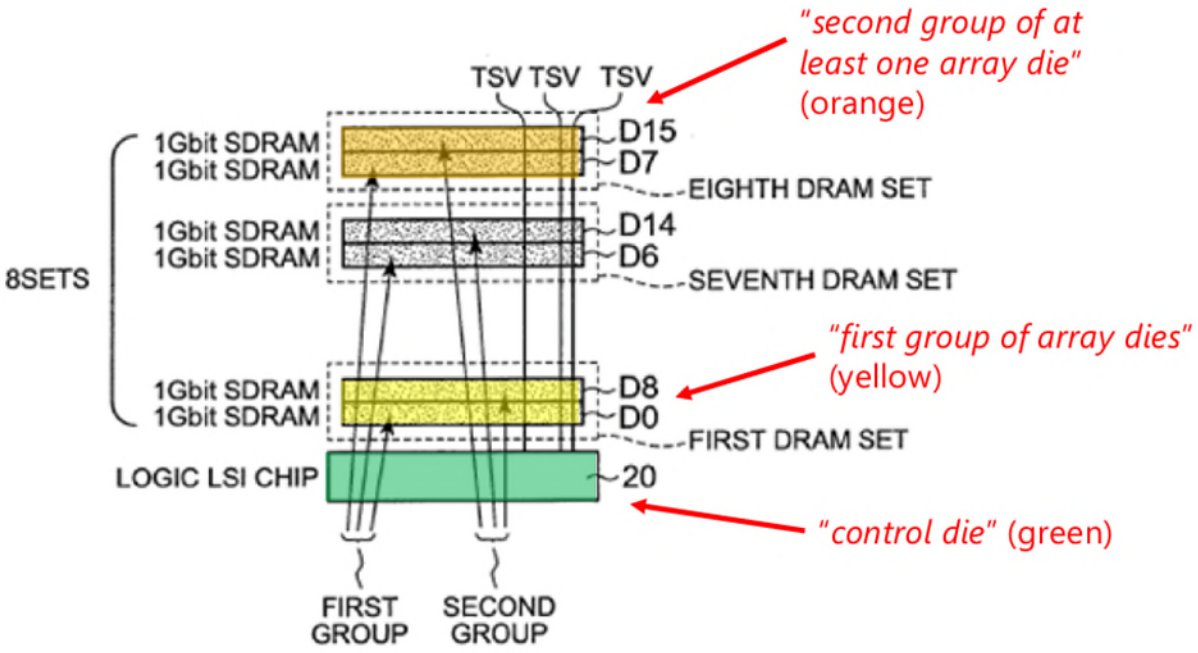
FIG. 4

e) ***[1.e.1] Control Die***

Ground 4 teaches "*a control die* [e.g., Riho's Logic LSI chip 20 (green), described as "a control chip"] *comprising*." EX1016, ¶[0026], Fig.1 (below);

EX1003, ¶¶745-752. As discussed above (pp.91-94), the "*control die*" in the combination of Ground 4 may emulate one or more characteristics, such as the number of ranks (e.g., for "rank multiplication"), that are different from the characteristics of the physical memory devices. EX1003, ¶750.

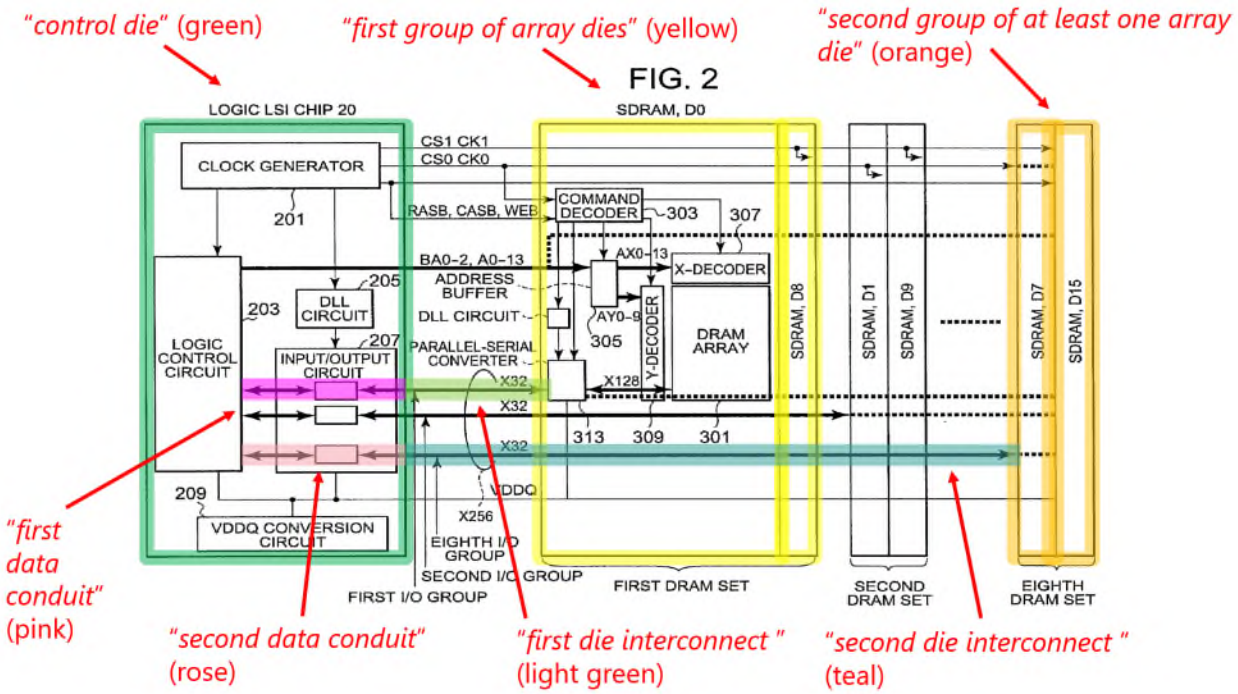
FIG. 1



f) ***[1.e.2] and [1.e.3] First and Second Data Conduit***

Ground 4 teaches "*at least a first data conduit* [(pink)] *between the first die interconnect* [DQ TSV08 (light green)] *and a first terminal of the plurality of input/output terminals* [from [1.b] (pp.95-98)]*, and at least a second data conduit* [(rose)] *between the second die interconnect* [DQ TSV715 (teal)] *and the first terminal, the first terminal being a data terminal* [e.g., an external data terminal of

the control chip 20 (green)]." EX1003, ¶¶753-769. In particular, Riho discloses "external terminals (not illustrated)" and that "logic circuit 203 provided in the logic LSI chip 20…sends and receives data signals DQ between itself and the input/output circuit 207," and refers to those data signals as an "I/O group," indicating that control chip 20 (green, below) has an external input/output "*data terminal*" for communicating data signals via "*data conduit[s]*" (pink, rose, below) to the array dies. EX1016, ¶¶[0026, 0039-40, 0045-46], Fig.2 (below); EX1003, ¶¶756-762.



Furthermore, as explained above (pp.91-94), a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system pursuant to the JEDEC standards, and Rajan discloses external

terminals for data signals (below) that comply with the JEDEC standards. EX1015, 2:6-7, 3:52-54, 4:20-24, 5:36-43, 8:8-11, Figs.4, 18 (below); EX1019, p.12; EX1035, p.2; EX1003, ¶¶763-766. Rajan also teaches that the "*first*" (pink) and "*second*" (rose) "*data conduit[s]*" would be coupled to the "*first terminal*" for data, as shown below. *Id.*; EX1003, ¶¶763, 766-767; *see also* pp.8-11, 29-30.

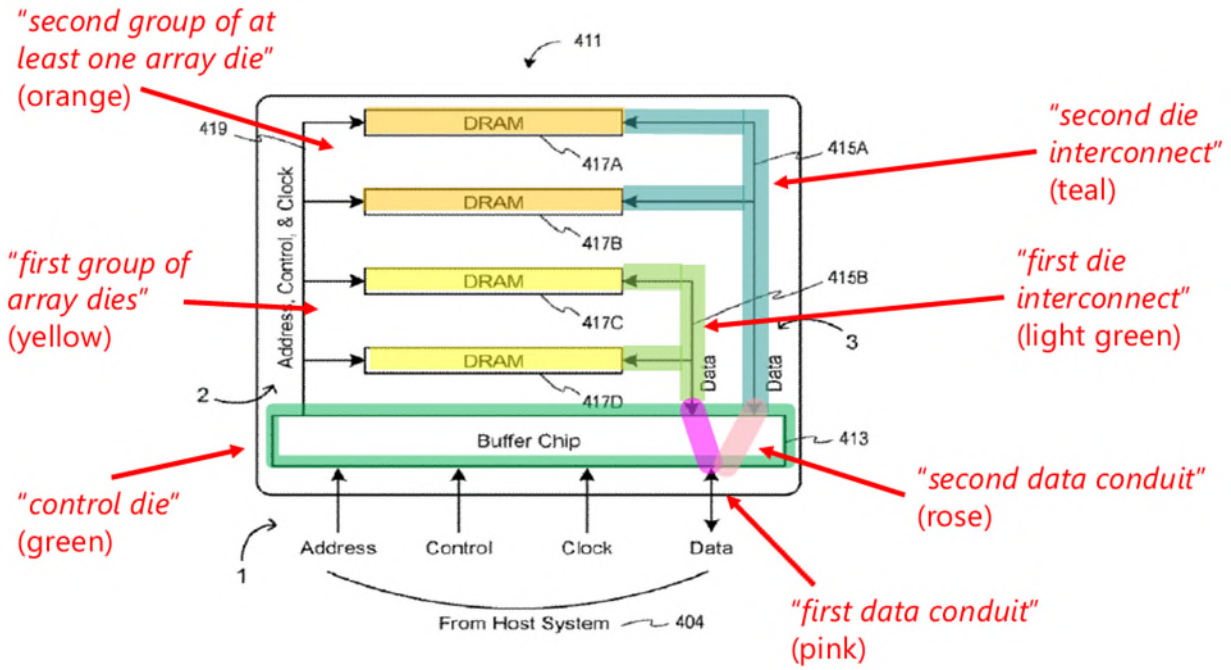


FIG. 4

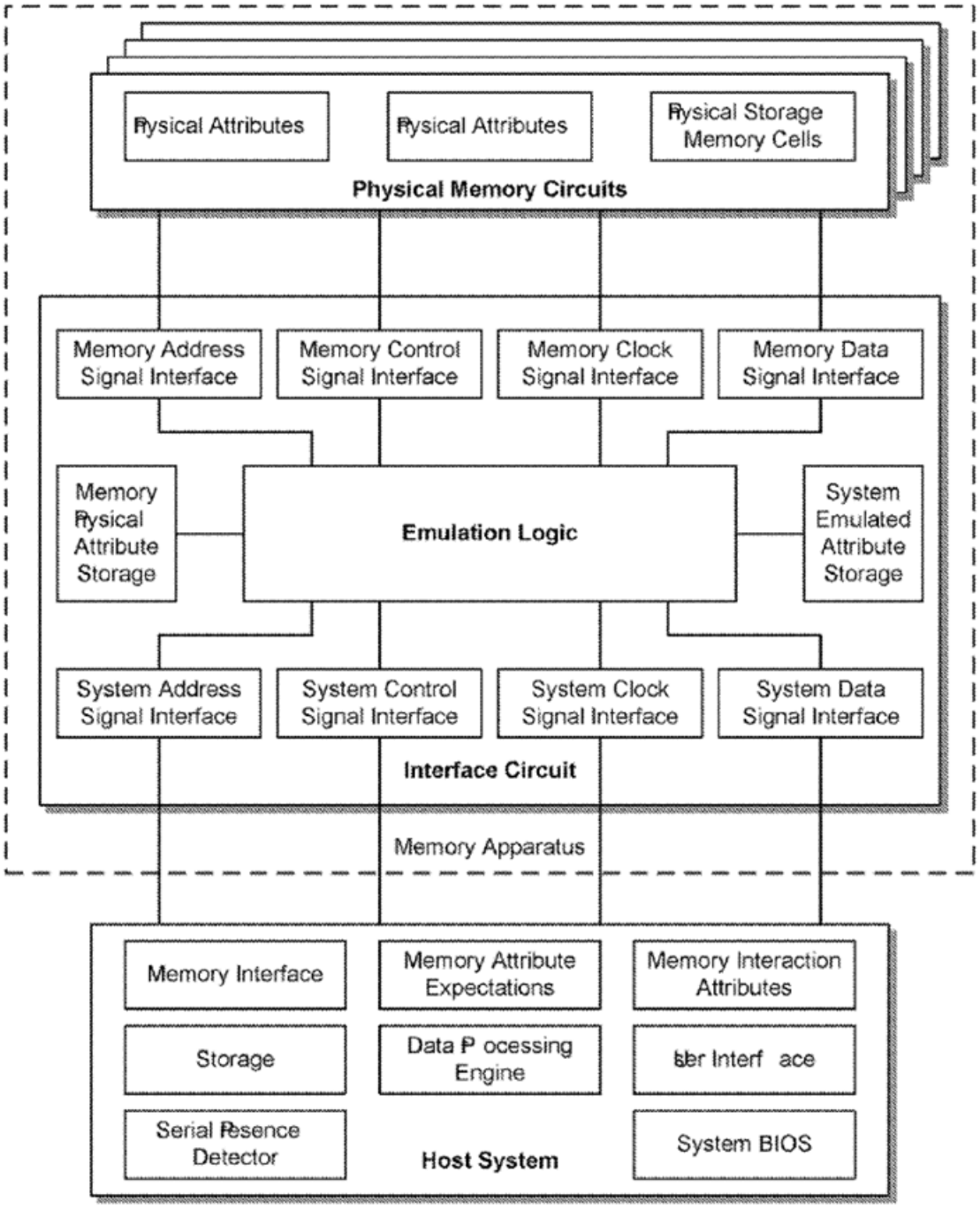
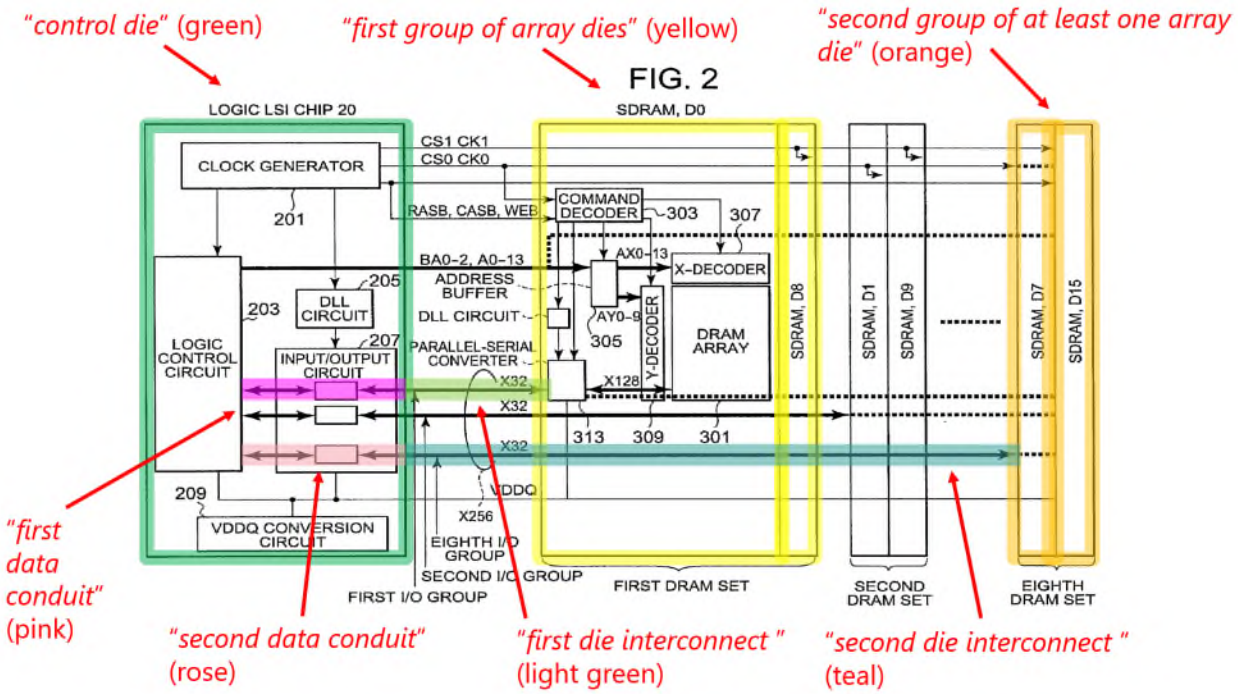


FIG. 18

g) ***[1.e.4] Control Circuit***

Ground 4 teaches "*the control die* [green] *further comprising a control circuit* [including logic control circuit 203 and control circuit in input/output circuit

207, which may emulate one or more characteristics, e.g., ranks, *supra* pp.8-11, 91-94] *to control respective states* [e.g., for communicating data in the read or write direction with the correct timing] *of the first data conduit* [pink] *and the second data conduit* [rose] *in response to control signals* [e.g., read/write command signals with chip-select signals pursuant to the JEDEC standard, EX1019, pp.6-14, 18, 33] *received via one or more second terminals of the plurality of terminals* [from [1.b] (pp.95-98)]." EX1016, ¶¶[0039-40, 0045, 0053], Fig.2 (below); EX1003, ¶¶770-778.



Furthermore, as explained above (pp.91-94), a POSITA would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system, and Rajan discloses external terminals for control signals to

read/write data according to the timing requirements in the JEDEC standards. EX1003, ¶¶773-774; EX1015, 11:12-12:13, Fig.14 (below, illustrating possible timings for read/write operations); EX1019, pp.13, 23-24 ("CAS latency"), 33.

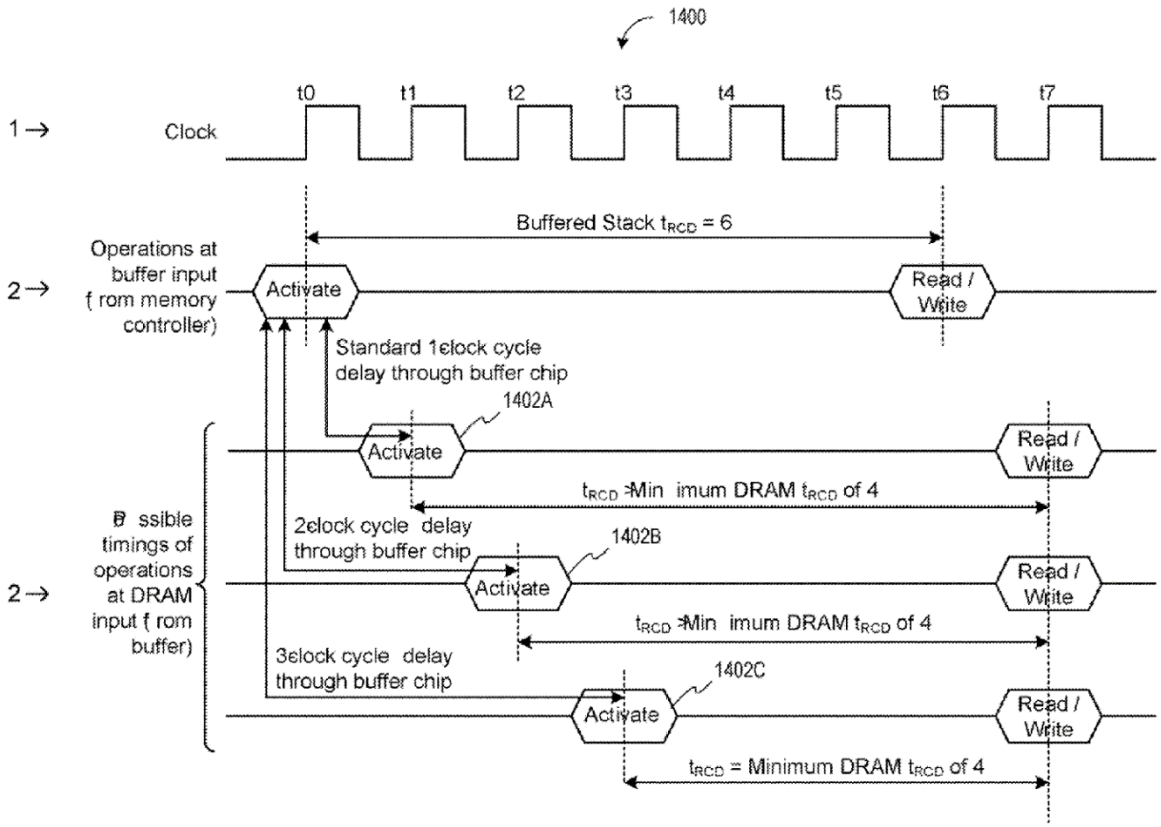


FIG. 14

3. Claim 2

For the same reasons discussed for [1.e.4] (pp.106-108), Ground 4 teaches "*claim 1, wherein the control signals* [from [1.e.4] (pp.106-108)] *include data path control signals* [e.g., read/write command signals, including chip-select signals pursuant to the JEDEC standard] *for controlling the first* [pink] *and second* [rose] *data conduits* [e.g., by controlling the timing and direction of the data transfer

(read or write) and selecting the die(s) for the data transfer (according to chip-select signals)]." EX1003, ¶¶779-786; *supra* pp.106-108. Moreover, in the combination of Ground 4, either the "*control circuit*" in the memory package and/or the register on the memory module external to the memory package can implement "rank multiplication," as discussed above (pp.8-11, 91-94), thus affecting the "*data path control signals*." EX1003, ¶784.

4. Claim 3

Ground 4 teaches "*claim 1, wherein the control circuit* [from [1.e.4] (pp.106-108)] *is configured to generate data path control signals* [*see* claim 2 (pp.108-109), e.g., internal read/write signals, including chip-select signals pursuant to the JEDEC standard] *for controlling the first* [pink] *and second* [rose] *data conduits* [*see* claim 2 (pp.108-109)] *in response to the received control signals* [from [1.e.4] (pp.106-108)]." EX1003, ¶¶787-798. As discussed above for claim 2, in the combination of Ground 4, the "*control circuit*" in the memory package can also implement "rank multiplication," as discussed above (pp.8-11, 91-94), thus generating "*data path control signals*." EX1003, ¶¶795-796; EX1015, 3:27-30, 6:30-7:67, Fig.18 (second below). In addition, as taught by Rajan, the "*control circuit*" can control the "*data conduits*" to emulate the timing and other characteristics of the JEDEC standard, as shown below. EX1015, 3:42-50, 9:46-

10:27, Fig. 10 (first below); EX1019, pp.23-24 ("CAS latency"); EX1003, ¶¶793-794.

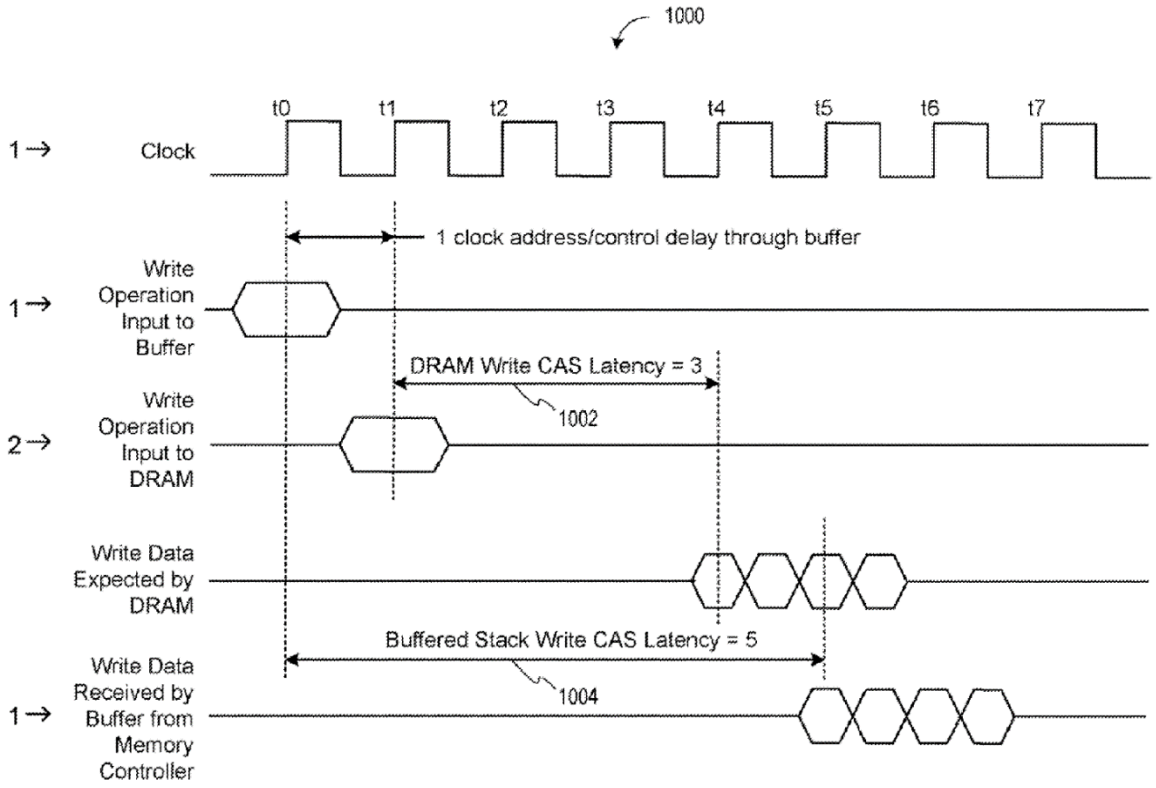


FIG. 10

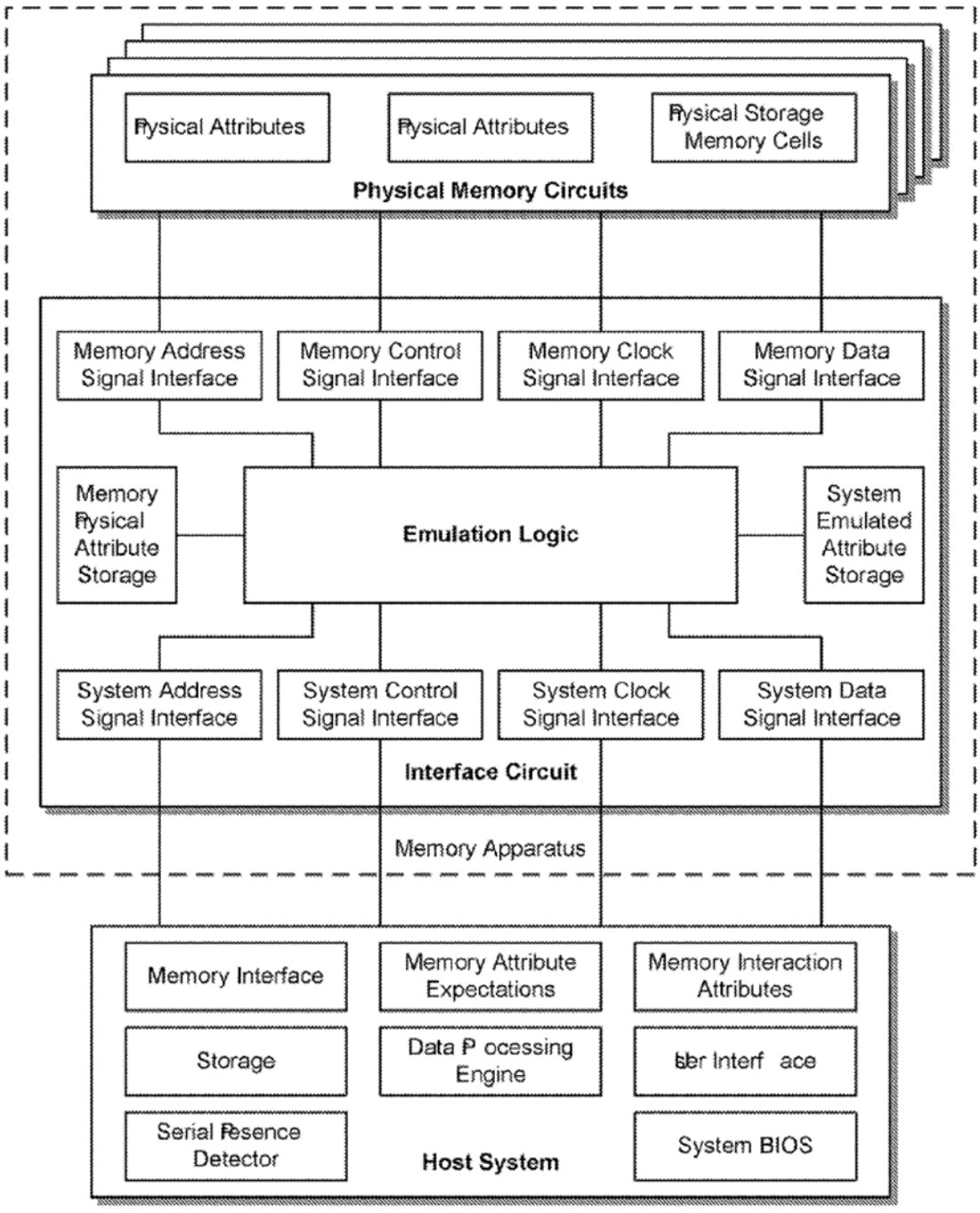

Physical Attributes
Physical Attributes
Physical Storage Memory Cells
Physical Memory Circuits
Memory Address Signal Interface
Memory Control Signal Interface
Memory Clock Signal Interface
Memory Data Signal Interface
Memory Physical Attribute Storage
Emulation Logic
System Emulated Attribute Storage
System Address Signal Interface
System Control Signal Interface
System Clock Signal Interface
System Data Signal Interface
Interface Circuit
Memory Apparatus
Memory Interface
Memory Attribute Expectations
Memory Interaction Attributes
Storage
Data Processing Engine
User Interface
Serial Presence Detector
Host System
System BIOS

FIG. 18

5. Claim 4

a) *[4.a] Command/Address Signals*

Ground 4 teaches "*[t]he memory package of claim 3, wherein the control signals* [from [1.e.4] (pp.106-108)] *include command/address signals* [e.g., read/write commands, which, as discussed for claim limitation [1.b] (pp.95-98), and in light of the JEDEC standards, EX1019, pp.6-14, 18, 33; EX1023, p.9, Fig.16; EX1022, pp.318-20, 332-35, would have been understood by a POSITA to include chip-select (CS) control signals and address signals (e.g., A0-A15) identifying where to store or retrieve the data] *and*." EX1003, ¶¶800-804; EX1015, Figs. 4, 18 (below); *see also* EX1019, p.13 (chip-select control signals are "considered part of the command code").

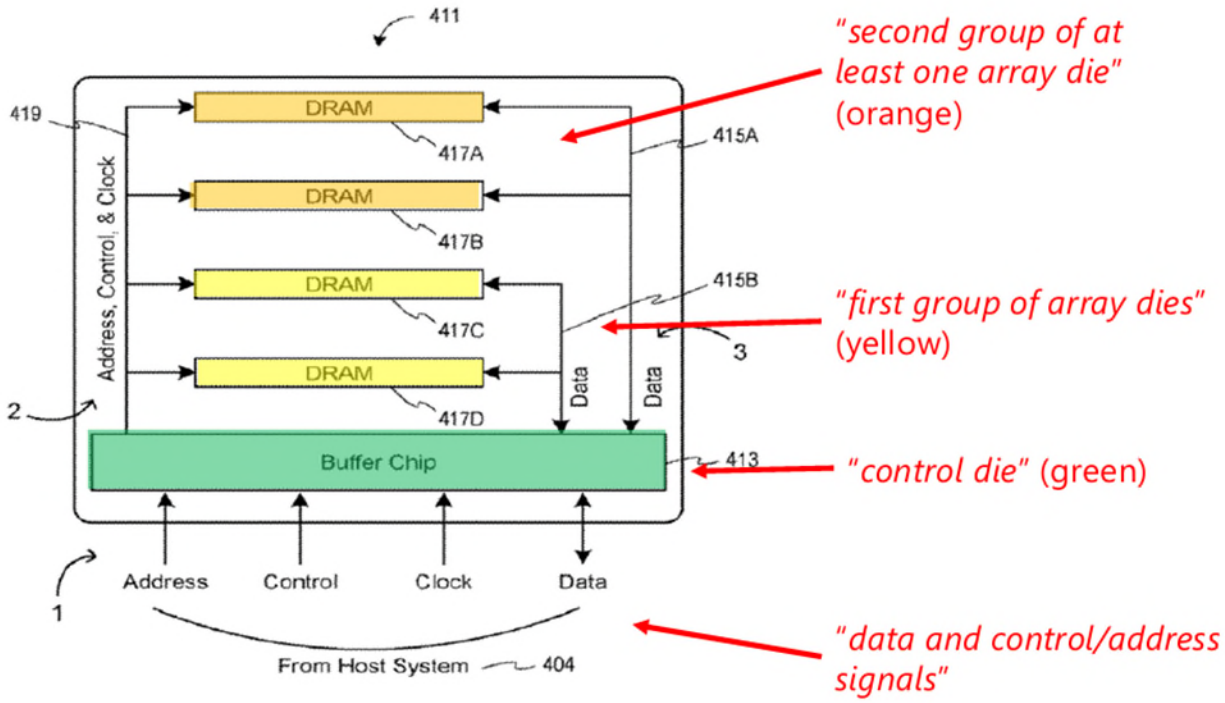

411
419
DRAM
417A
DRAM
417B
DRAM
417C
DRAM
417D
Address, Control, & Clock
415A
415B
Data
Data
3
2
Buffer Chip
413
1
Address
Control
Clock
Data
From Host System
404
"second group of at least one array die" (orange)
"first group of array dies" (yellow)
"control die" (green)
"data and control/address signals"

FIG. 4

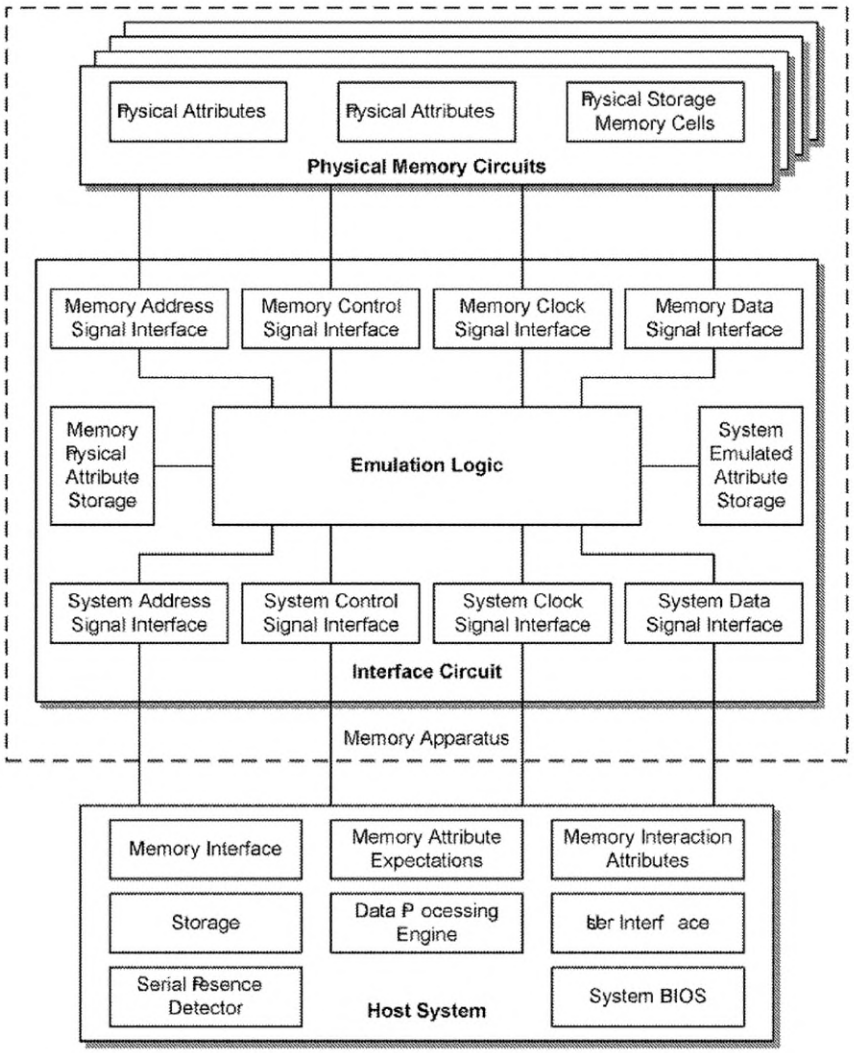
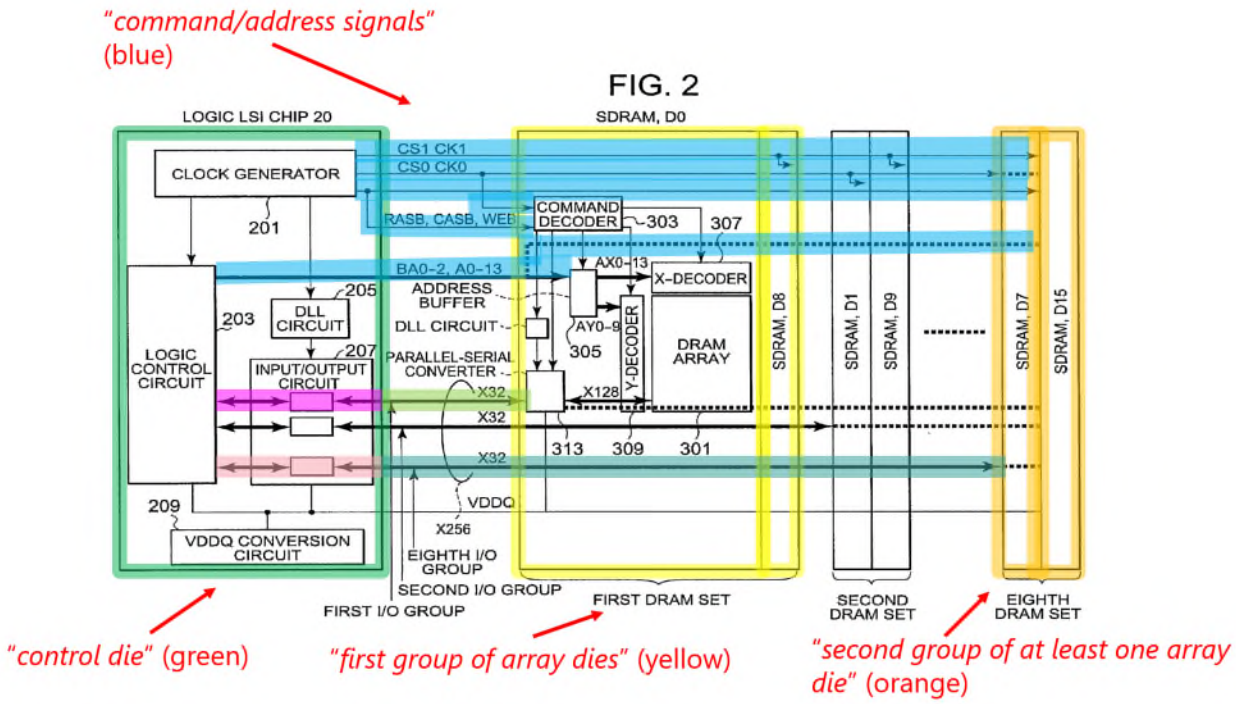


FIG. 18

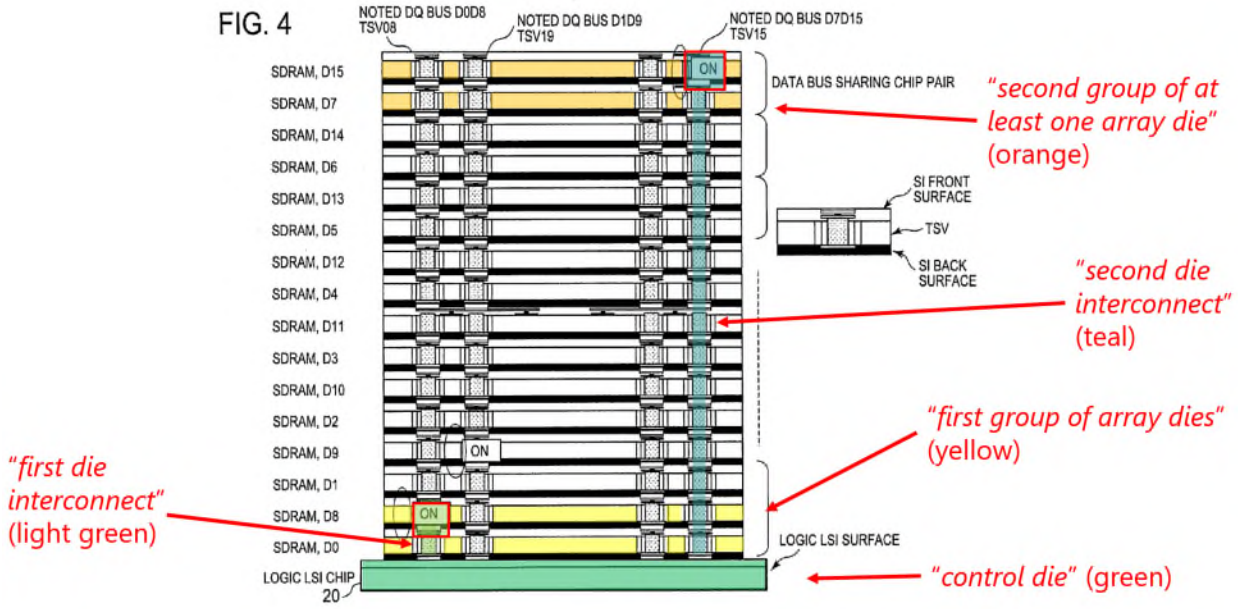
b) ***[4.b] Control Die Configured to Provide Command/Address Signals***

Ground 4 teaches "*wherein the control die* [green] *is configured to provide the command/address signals* [from [4.a] (pp.112-114), such as CS0CK0, CS1CK1, RASB, CASB, WEB, BA0-2, A0-13 (blue, below)] *to the plurality of stacked array dies* [e.g., D0-D15, yellow, orange]." EX1016, ¶¶[0038, 0043], Fig.2 (below); EX1003, ¶¶805-810.



6. Claim 5

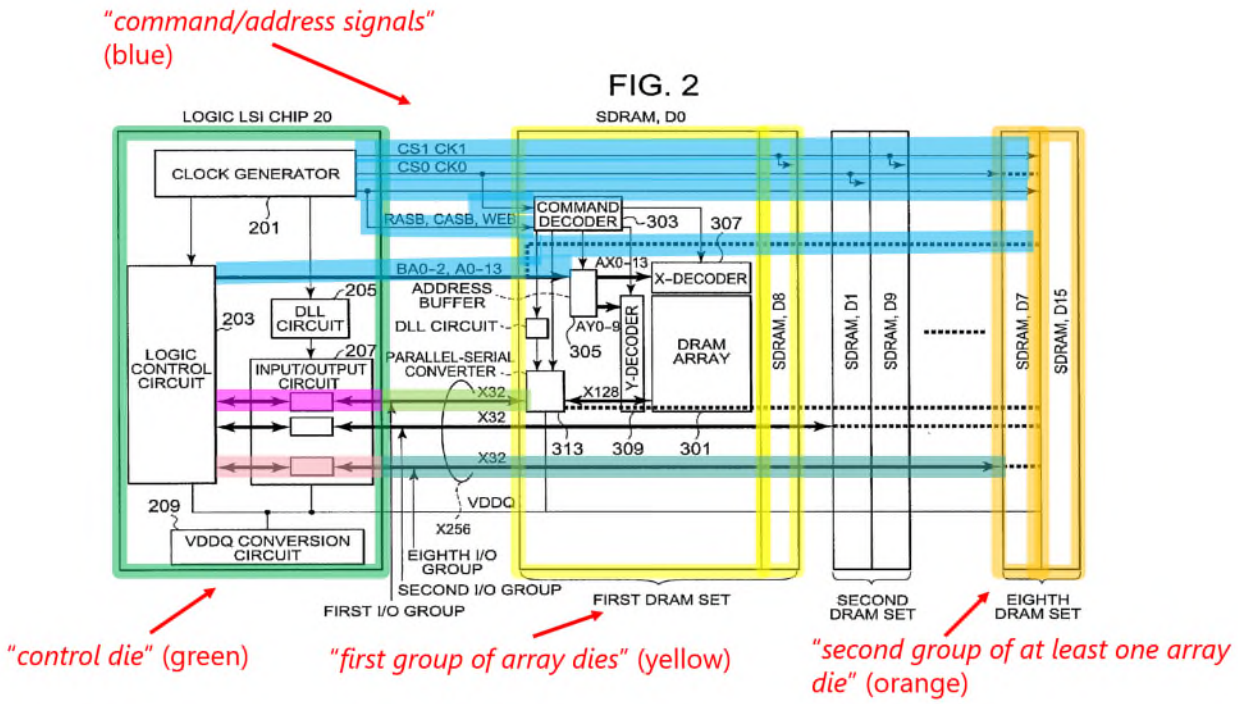
Ground 4 teaches "*[t]he memory package of claim 1, wherein the first die interconnect* [light green] *comprises a first through-silicon via* [e.g., Riho's TSV08] *and wherein the second die interconnect* [teal] *comprises a second through-silicon via* [e.g., Riho's TSV715]." EX1016, ¶¶[0030, 0063-64], Fig.4 (below); EX1003, ¶¶811-816.



7. Claim 6

a) *[6.a] Chip-Select Conduits*

Ground 4 teaches "*[t]he memory package of claim 1, wherein the control die* [green] *further comprises chip-select conduits* [e.g., for conducting chip-selection signals CS0CK0 and CS1CK1 (blue, below)]*, the memory package further comprising*." EX1016, ¶[0033], Fig.2; EX1003, ¶¶818-826; *see also infra* pp.129-130 (claim 12).



Moreover, in the combination of Ground 4, it would be obvious to use "*chip-select conduits*" to transmit generated chip-select signals to corresponding "*array dies*" to emulate the JEDEC standard (e.g., for "rank multiplication," pp.8-11, 91-94). EX1015, 3:27-30, 6:30-7:67; EX1003, ¶823. Furthermore, it would be obvious to use drivers (e.g., in the "*chip-select conduits*") to properly transmit the chip-select signals from the "*control die*" to the respective "*array dies*." *Supra* pp.6-8; EX1003, ¶824. Indeed, the "chip-select bus … is essential in a JEDEC style memory system." EX1022, p.319; EX1019, pp.12-13, Fig.2 (below).

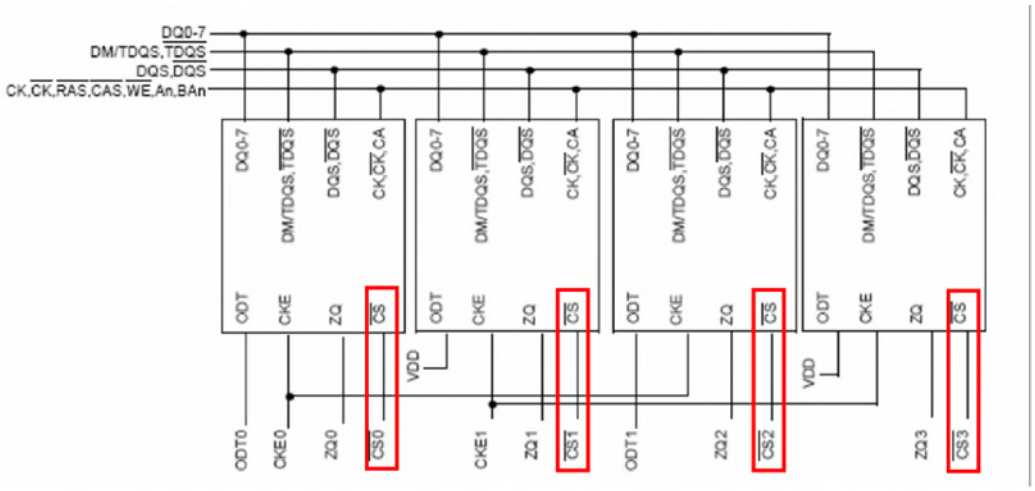
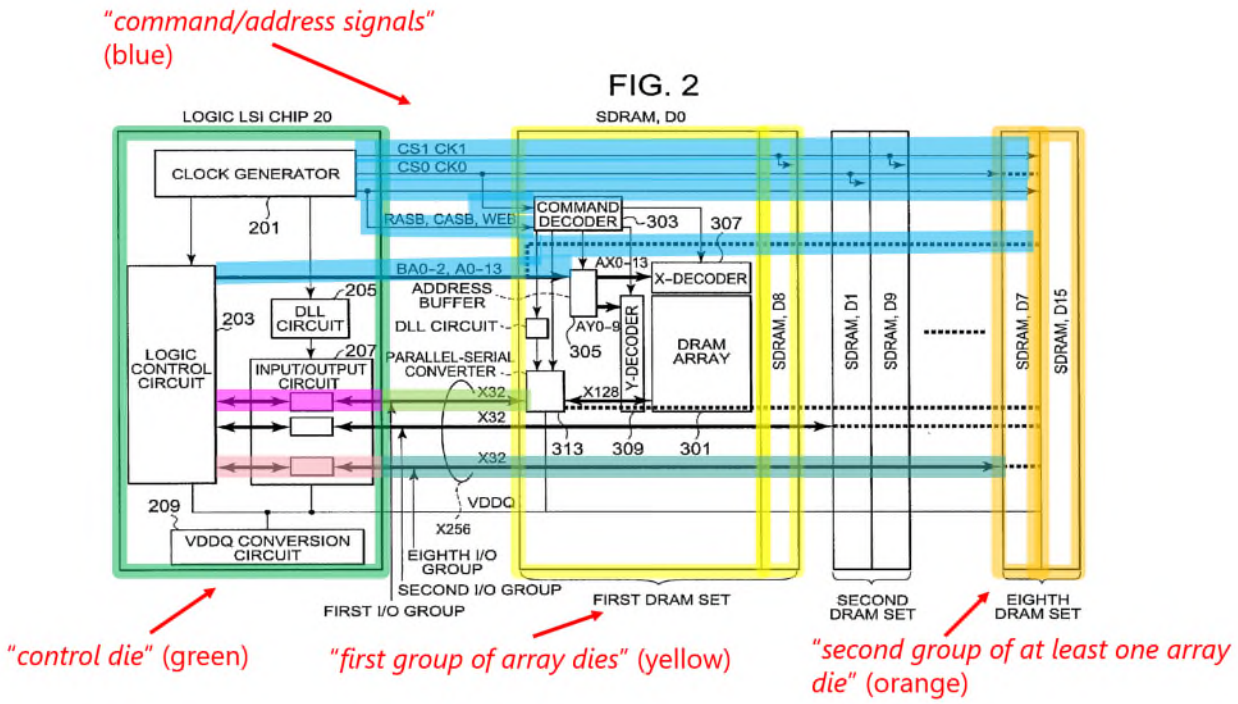


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

b) ***[6.b] Third Die Interconnects***

Ground 4 teaches "*third die interconnects* [e.g., Riho's "TSVs" for "CS0CK0 and CS1CK1" and "command signals" (blue, below), EX1016, ¶[0038]] *coupled between respective chip-select conduits* [from [6.a], above] *and respective ones of the plurality of stacked array dies* [yellow, orange]." EX1003, ¶¶827-832. The 060 Patent also admits that transmitting separate chip-select signals through "*die interconnects*" to select an "*array die*" was well-known at the time. EX1001, 1:49-56, Figs.1A-1B; EX1003, ¶830.

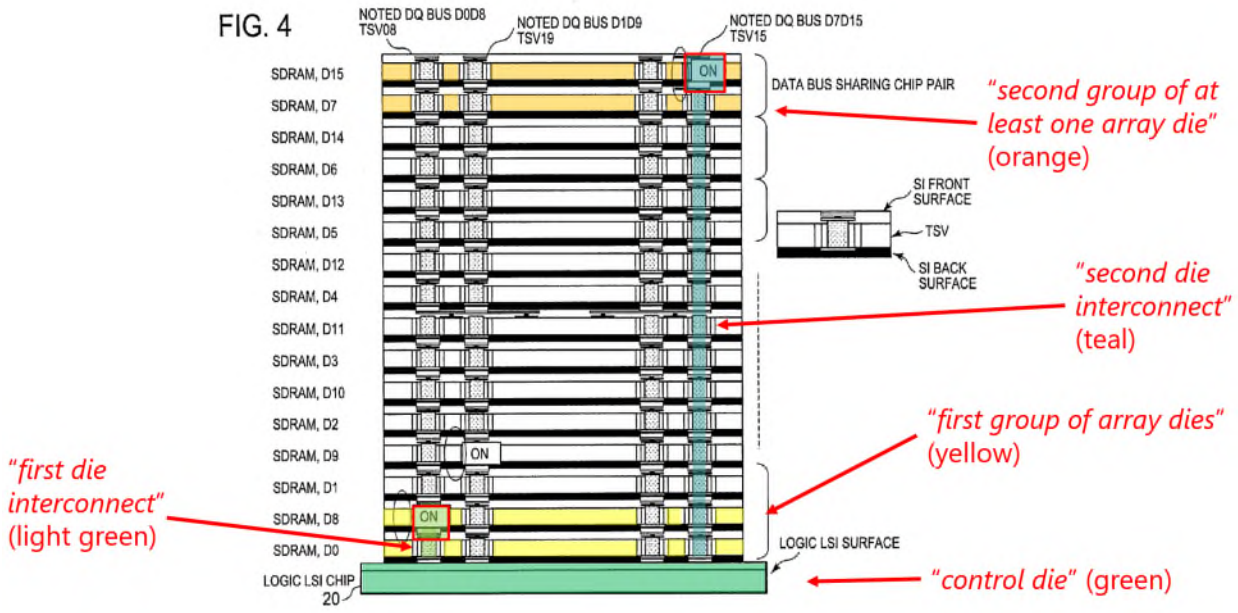


8. Claim 7

a) *[7.a] First and Second Number of Array Dies*

Ground 4 teaches "*[t]he memory package of claim 1, wherein a first number of* [two] *array dies in the first group of array dies* [(yellow, below) sharing a data signal TSV] *and a second number of at least one array die* [two dies] *in the second group of at least one array die* [(orange, below) sharing another data signal TSV] *are selected in consideration of a load of the first die interconnect and a load of the second die interconnect* [including the load of each of the data signal TSVs, *see* EX1016, ¶¶[0103, 0119-20]] *so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit* [so the "skew between data signals DQ and data strobe signals DQS/B can be minimized" allowing a "single synchronization signal with high accuracy," EX1016, ¶[0050,

0053-54]]." EX1003, ¶¶834-842; *see also supra* pp.6-8 (more load creates more delay); EX1019, p.13 ("Data Strobe" for reads and writes).



b) ***[7.b] First and Second Load***

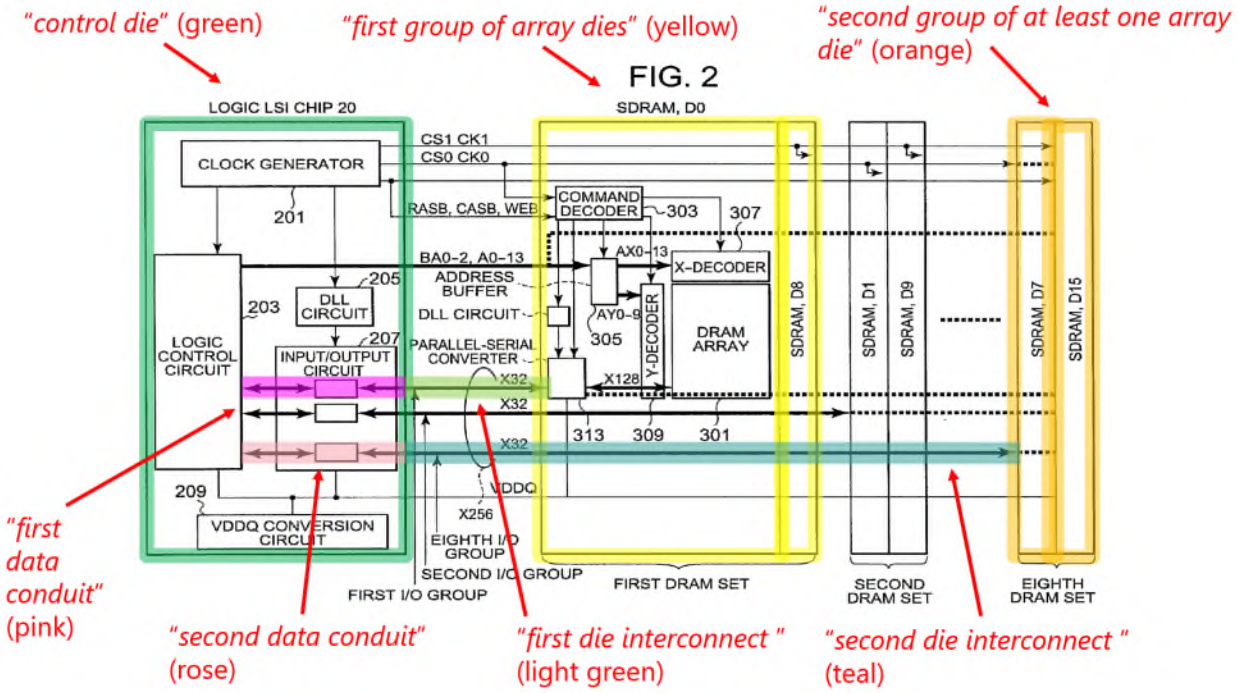
Ground 4 teaches "*the first load including a load of the first die interconnect* [(light green, above) from Riho's data signal DQ TSV08]*, and a load of the first group of array dies* [(yellow, above) including pair of SDRAM chips D0/D8]*, and the second load including a load of the second die interconnect* [(teal, above) from data signal DQ TSV715] *and a load of the second group of at least one array die* [(orange, above) including pair of SDRAM chips D7/D15]." EX1016, ¶¶[0013, 0119-20, 0132]; EX1003, ¶¶843-849. A POSITA would have understood from Riho's disclosure that the load for driving the data signals includes the loads of the

interconnecting vias and of the SDRAMs coupled to those vias. *Id.*; *supra*, pp.6-8; EX1003, ¶847.

9. Claim 8

a) ***[8.a] Data Path Control Signals***

Ground 4 teaches "*[t]he memory package of claim 1, wherein the respective states* [from [1.e.4] (pp.106-108)] *of the first data conduit* [(pink) connected to TSV08] *and the second data conduit* [(rose) connected to TSV715] *are controlled by one or more data path control signals* [see claims 2-3 (pp.108-111)]." EX1003, ¶¶851-855.



b) ***[8.b] Control Die is Configurable***

(1) [8.b.1] First and Second Mode

Ground 4 teaches "*wherein the control die is configurable to operate in any one of a first mode* [e.g., where the number and type of memory devices is known to the external controller, so the control "signals may pass through [the '*control die*'] unaltered," *see* [8.b.2] below] *and a second mode* [e.g., where the control signals are "altered" by the "*control die*" to emulates other characteristics, such as timing parameters and the number and type of memory devices in the stack, *see* [8.b.3] below]*, and wherein*." EX1015, 6:30-38, 14:51-62, Fig.18 (below, showing emulation logic); EX1003, ¶¶856-863. A POSITA would have been motivated to implement Rajan's different modes of interface operation to make Riho's memory stack compatible with host systems having different memory attribute expectations and memory interaction attributes. *Supra* pp.91-94; EX1003, ¶861.

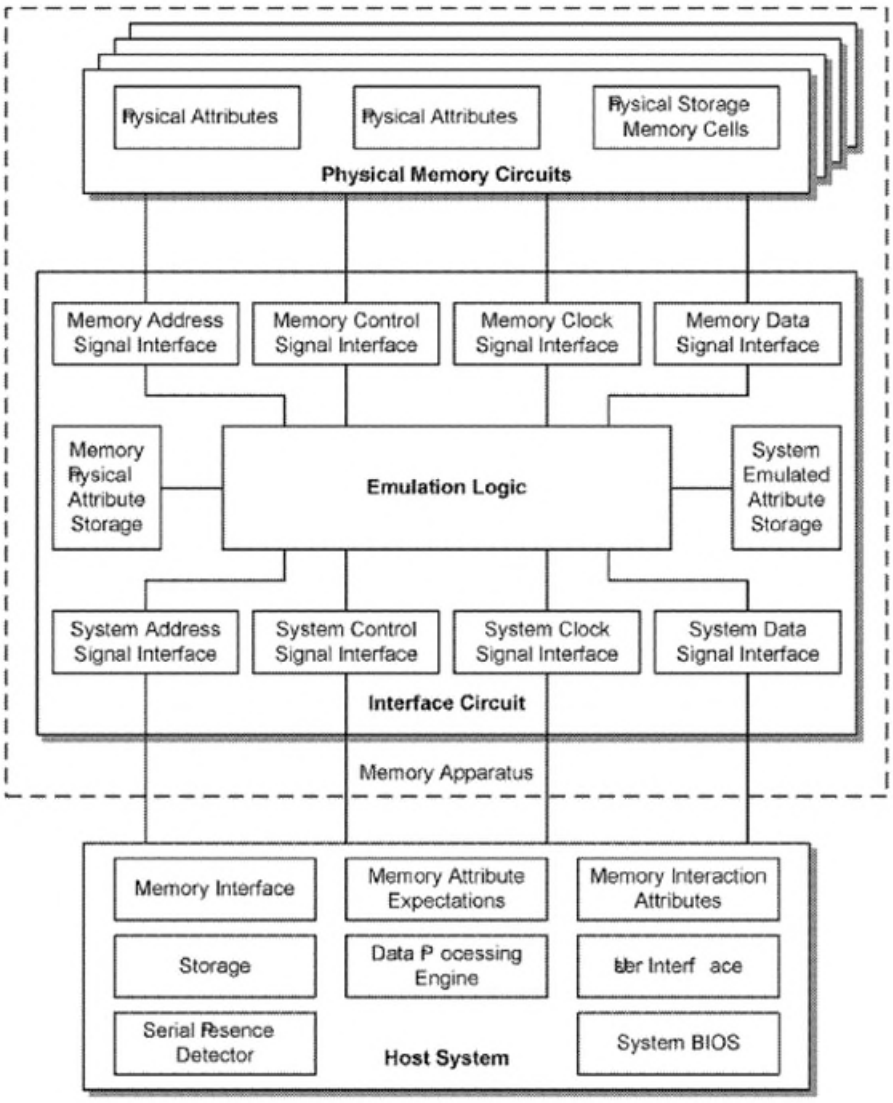


FIG. 18

(2) [8.b.2] First Mode

As explained for claim 2 (pp.108-109), Ground 4 teaches "*in the first mode, the control die receives the data path control signals* [e.g., read/write commands including chip-select signals] *from the one or more external devices*." EX1003, ¶¶864-868.

(3) [8.b.3] Control Die Generates Control Signals

Ground 4 teaches "*in the second mode* [e.g., Rajan's interface implemented in Riho's control chip emulating an interface with, e.g., different timing or different number and/or type of memory chips]*, the control die generates the data path control signals* [see claim 3 (pp.109-111), e.g., including internal control signals for controlling direction (read or write) and timing of, and selecting the die(s) for, data transfer through input/output circuit 207] *from at least some of the control/address signals received from the one or more external devices*." EX1003, ¶¶869-875. For example, Rajan's emulation logic can generate chip-select signals (e.g., for "rank multiplication," pp.8-11, 91-94) "*from at least some of the control/address signals received from the one or more external devices*," EX1015, 7:4-67, Fig.18; EX1003, ¶872, and Rajan's emulation logic can generate delayed read/write commands used to control the direction and timing of data transmissions, EX1015, 3:52-58, 9:46-10:27, Fig.11 (below); EX1003, ¶873.

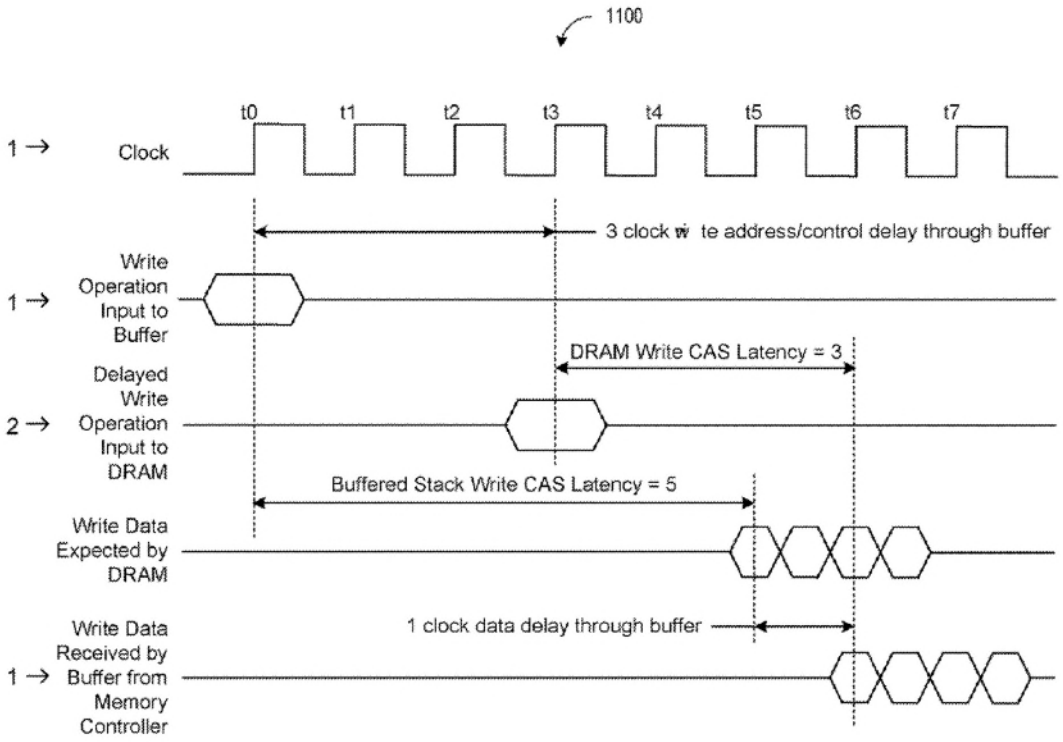
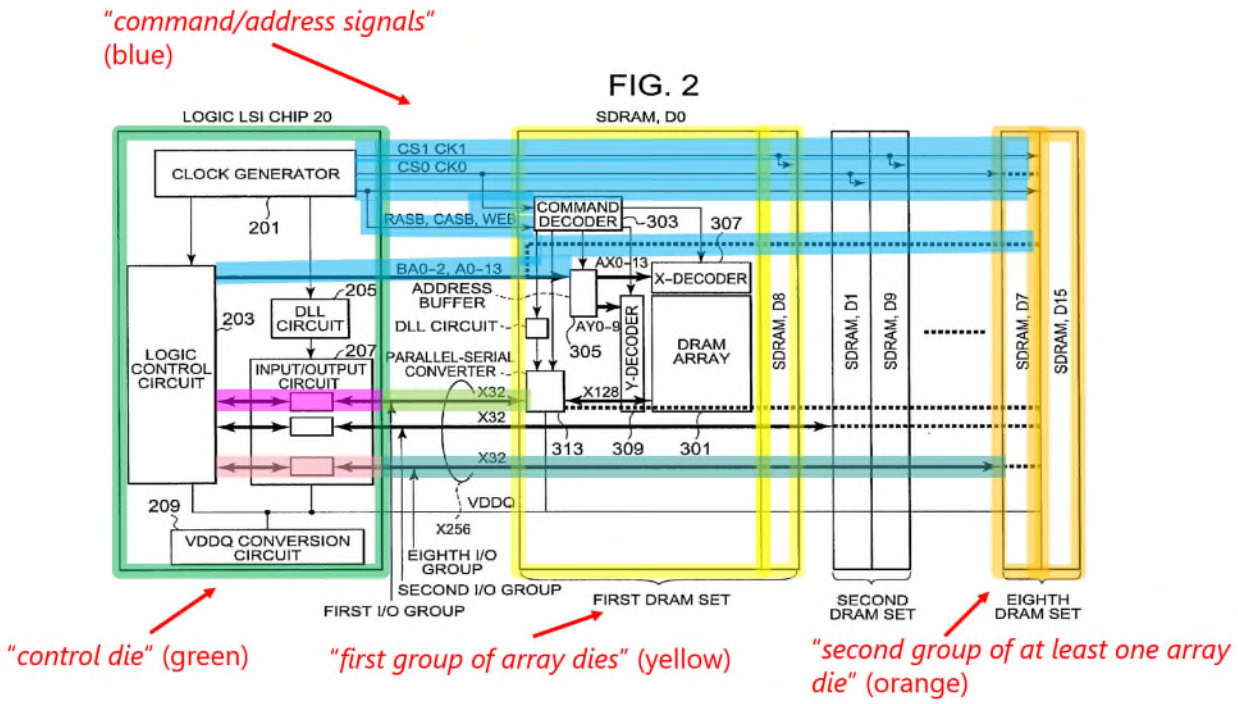


FIG. 11

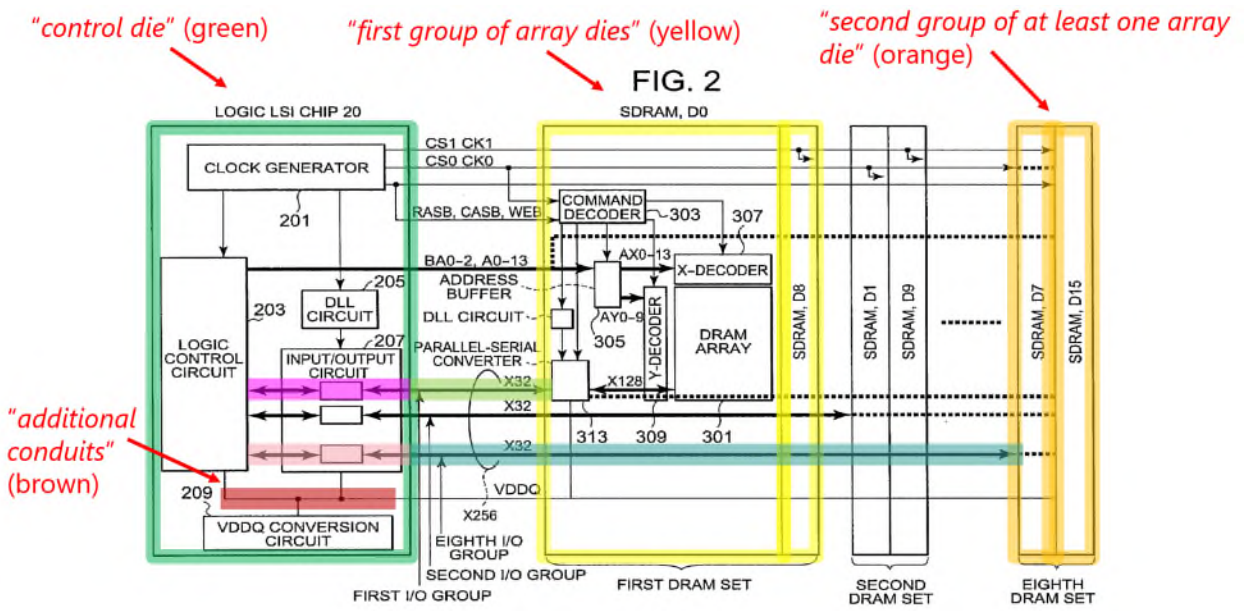
10. Claim 9

Ground 4 teaches "*[t]he memory package of claim 1, wherein the control die* [green] *further comprises command/address conduits* [e.g., connecting clock generator 201 and logic control circuit 203 in control chip 20 to corresponding "TSVs…[for] address, command," EX1016, ¶¶[0030, 0034, 0037-39, 0043-44]] *configured to provide corresponding command/address signals* [(blue, below)] *to the array dies* [SDRAM chips D0-D15 (yellow, orange, below)]*, the command/address signals including at least one memory cell address* [in respective DRAM array 301, *see* EX1016, ¶[0049]; EX1019, p.13 ("A0-A15")]," as further discussed for claim 4 (pp.112-115). EX1003, ¶¶876-882.



11. Claim 10

Ground 4 teaches "*[t]he memory package of claim 1, wherein the control die further comprises one or more additional conduits* [(brown, below) from VDDQ conversion circuit 209] *configured to provide one or more of a supply voltage signal and a ground signal to the array dies* [SDRAM chips D0-D15 (yellow, orange)]," *e.g.*, to power the operation of the memory chips (yellow, orange), including read/write operations. EX1016, ¶[0036], Fig.2 (below); EX1003, ¶¶883-890. A POSITA would have understood that a "*supply voltage*," e.g., VDDQ, would also require a corresponding "*ground signal*" to close the circuit, as standardized by JEDEC, EX1019, p.14. EX1003, ¶888.



12. Independent Claim 11

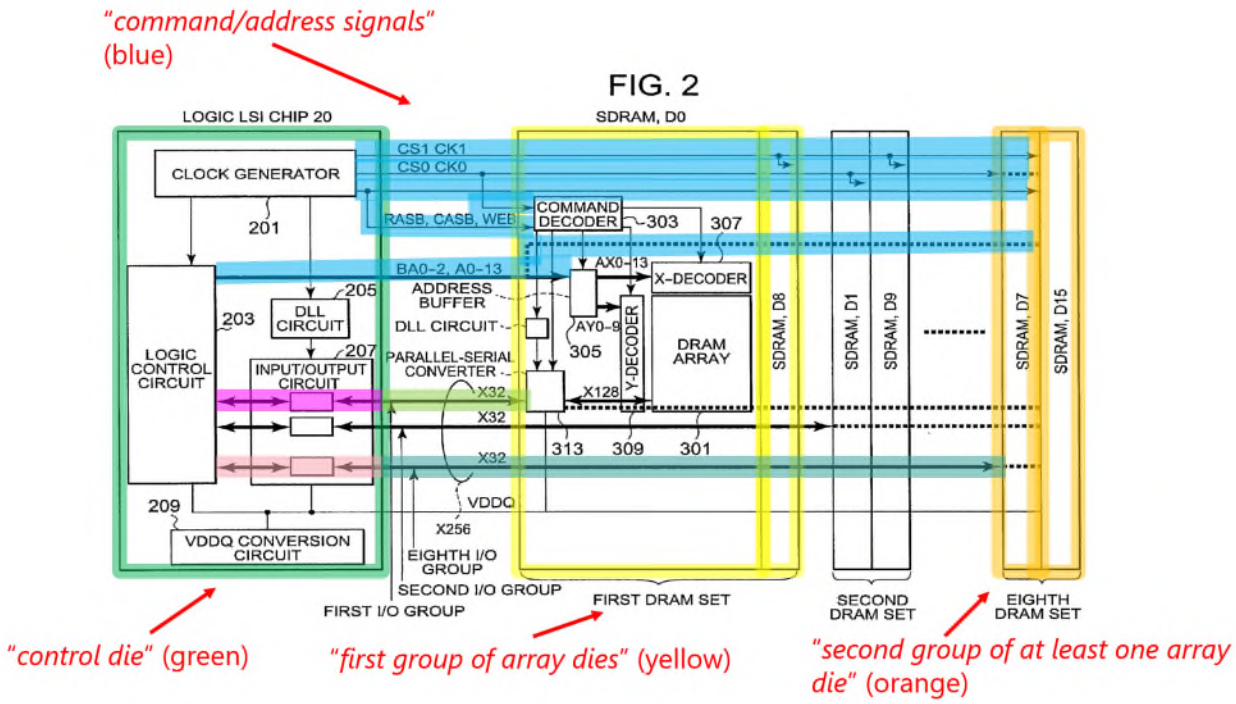
The limitations of claim 11 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 4 for at least the same reasons discussed above:

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[11.a]	[1.a]	¶¶892-894 (¶¶706-710)
[11.b]	[1.b]	¶¶895-898 (¶¶711-718)
[11.c]	[1.c]	¶¶899-902 (¶¶719-726)
[11.d.1]-[11.d.2]	[1.d.1]-[1.d.2]	¶¶903-906 (¶¶727-744)
[11.e.1]	[1.e.1]	¶¶907-910 (¶¶745-752)

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[11.e.2]-[11.e.3]	[1.e.2]-[1.e.3][11]	¶¶911-914 (¶¶753-769)
[11.e.4]	[6.a]-[6.b]	¶¶915-918 (¶¶818-832)
[11.e.5]	[1.e.4] and directly below	¶¶919-928 (¶¶770-778)

For [11.e.5], Ground 4 further teaches "*driv[ing] a data signal to an array die* [*see, e.g.*, Riho's description of "[e]ach input/output circuit 207 send[ing] and receiv[ing] 32-bit width data signals DQ between itself and the SDRAMs D0 and D15 [(yellow, orange, below)]," EX1016, ¶[0040]] *selected by at least one of the chip-select signals* [e.g., "CS0CK0" and "CS1CK1" (blue, below), EX1016, ¶[0033]; *see also* EX1015, 6:30-38; EX1022, pp.318-321; EX1023, pp.2-4, 9, Fig.16]." EX1003, ¶¶923-926.

[11] As explained below for [15.a] (pp.140-141), it would also be obvious for the first and second data conduits to each include a respective driver. EX1003, ¶¶950-962.

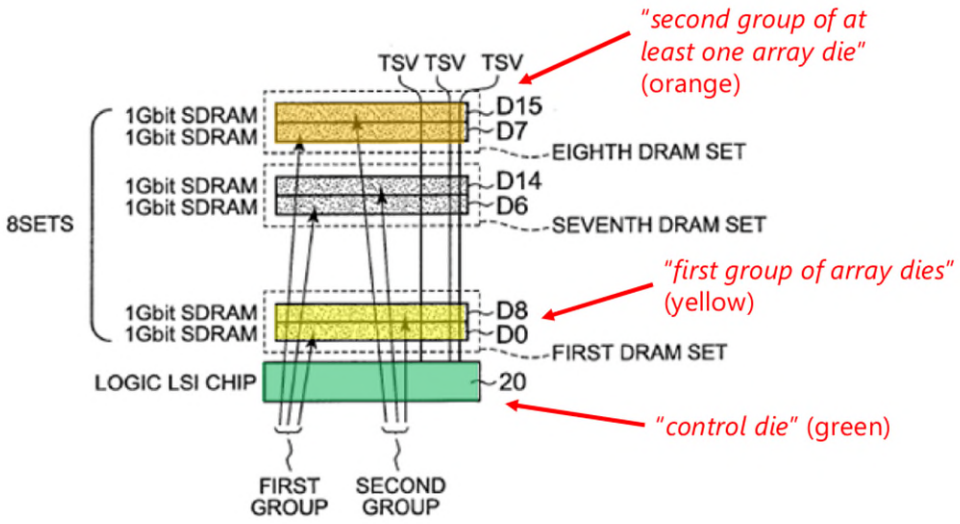


13. Claim 12

Ground 4 teaches "*[t]he memory package of claim 11, wherein the chip select conduits pass through the control die* [green]," as shown by Riho's disclosure of "external terminals" on the "lower side" of the "*control die*" (green, below) and that "I/O signal lines penetrating through the controlled chips [e.g., SDRAMs D0-D8, D7-D15 (yellow, orange)]…are connected to logic LSI chip 20 [green, below] and not directly to external terminals." EX1016, ¶[0026], Fig.1 (below); EX1003, ¶¶929-935. The 060 Patent also admits this was taught by the prior art, EX1001, 18:15-17, 19:55-56, consistent with the JEDEC standards, EX1019, pp.6-11 ("CS" terminals at bottom of "stacked" packages); EX1021,

pp.1-2 (MO-207 JEDEC standard with solder balls at the bottom of the package, below); EX1022, pp.374 ("BGA"), 476 ("FBGA").

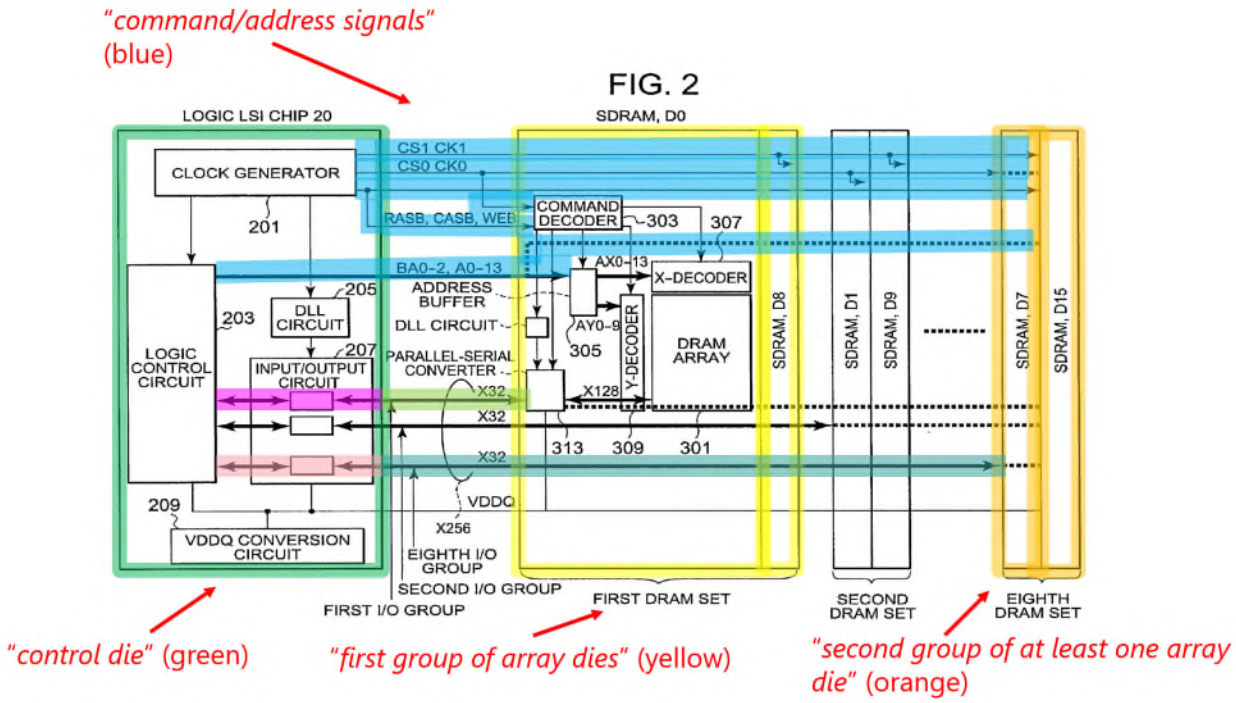
FIG. 1



14. Claim 13

Ground 4 teaches "*[t]he memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies.*" EX1003, ¶¶936-943. As discussed for [6.a] (pp.116-118), Ground 4 teaches "*chip select conduits*" that, as further discussed for [6.b] (pp.118-119), transmit chip-select signals up to the "*array dies*" above the "*control die*." Drivers were well-known (pp.6-8), and it would be obvious to a POSITA from Riho's disclosure that "clock generator 201 supplies" "CS0CK0" and "CS1CK1" to the "SDRAMs" to use "*drivers*" in the "*conduits*" to produce enough current to transmit each chip-select signal from one chip ("*control die*") to another chip

("*array die*"). EX1016, ¶[0037]; EX1030, pp.135-36 ("buffers are…used when high current flow is needed to drive external devices"); EX1038, p.68 ("tri-state drivers" are "commonly used"); EX1017, 1:14-20; EX1003, ¶941.



15. Claims 14, 16-19

The limitations of claims 14 and 16-19 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 4 for at least the same reasons discussed above:

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[14]	[5]	¶¶944-948 (¶¶811-816)

This limitation in claim 11…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[16]	[1.e.4], [8.b.3][12]	¶¶972-979 (¶¶770-778, 869-875)
[17]	[1.e.4], [4.a]-[4.b]	¶¶980-984 (¶¶770-778, 799-810)
[18]	[2], [4.a]-[4.b]	¶¶985-989 (¶¶779-786, 799-810)
[19.a]	[1.e.4], [3], [4.a], [8.b.3]	¶¶991-994 (¶¶770-778, 787-798, 800-804, 869-875)
[19.b]	[1.e.4], [3]	¶¶995-998 (¶¶770-778, 787-798)

16. Independent Claim 29

a) ***[29.a] Memory Module***

Ground 4 teaches "*[a] memory module* [e.g., including Riho's stacked memory devices, EX1016, ¶¶[0002-04], implemented in Rajan's DIMM memory module, EX1015, 1:28-32, 8:52-54, 15:3-12, Fig.8 (first below), e.g., to allow Riho's devices to be used in host systems with JEDEC-standard DIMM sockets] *operable via a memory control hub* [e.g., which may be part of Rajan's "memory controller (not shown)," EX1015, 3:5-7]." EX1003, ¶¶1089-1097; *see also* EX1022, pp.316-20 (describing "memory controller" for JEDEC-compliant systems), Fig.7.2 (second below); EX1037, Fig.1, 1:34-39 ("Memory Controller Hub (MCH)").

[12] *See also* note 3 on p.74. EX1003, ¶977.

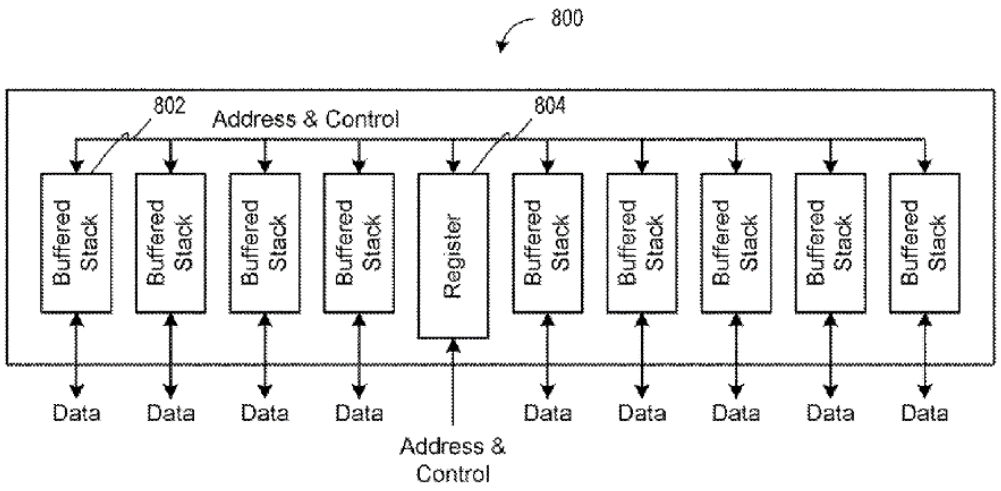


FIG. 8

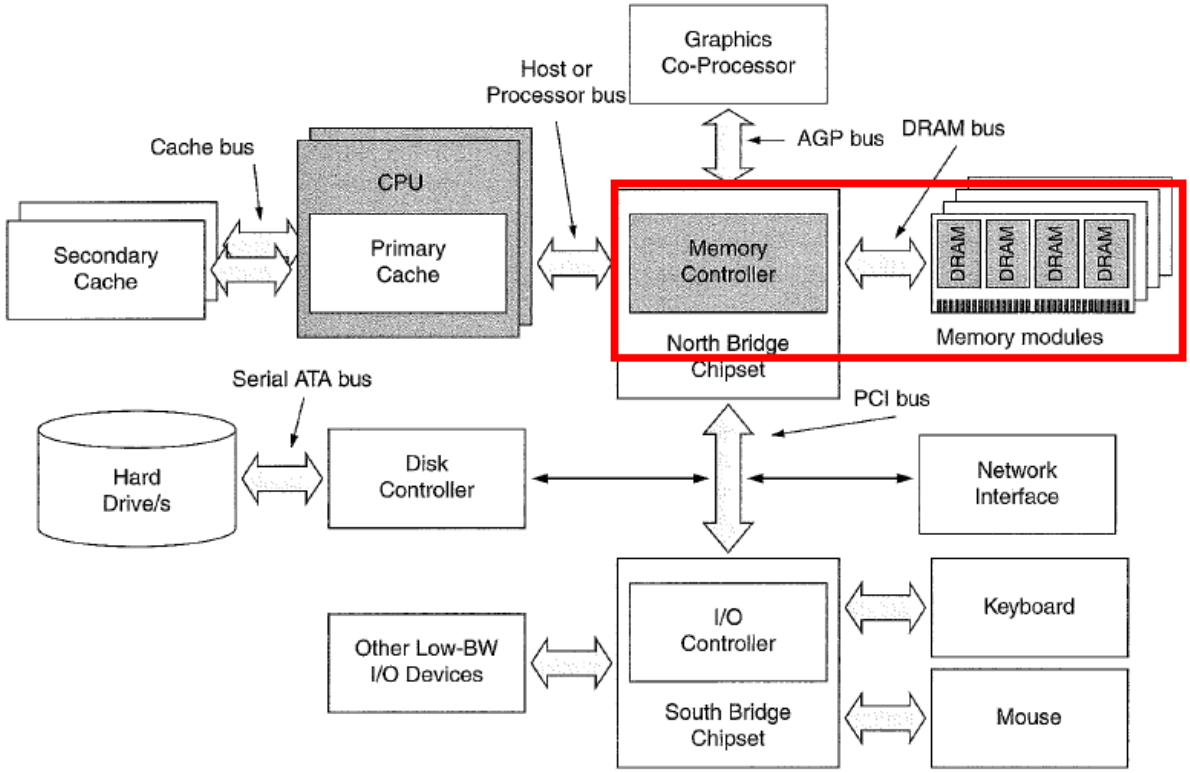


FIGURE 7.2: A typical PC organization. The DRAM subsystem is one part of a relatively complex whole. This figure illustrates a two-way multi-processor, with each processor having its own dedicated secondary cache. The parts most relevant to this report are shaded in darker grey: the CPU, the memory controller, and the individual DRAMs.

b) ***[29.b] Register Device***

Ground 4 teaches "*a register device* [e.g., Rajan's register 804, *see* EX1015, 8:52-58, Fig.8 (below)] *configured to receive command/address signals* [*see id.*; claim [4.a] (pp.112-114)] *from the memory control hub* [from [29.a] above] *and to generate control signals* [e.g., Rajan's register generating "Address & Control" signals (below), *see also* claim 30 (p.135)]." EX1003, ¶¶1098-1103, 1142-1149; *see also* EX1022, pp.43-44, 418-19 ("Registered Memory Module (RDIMM)").

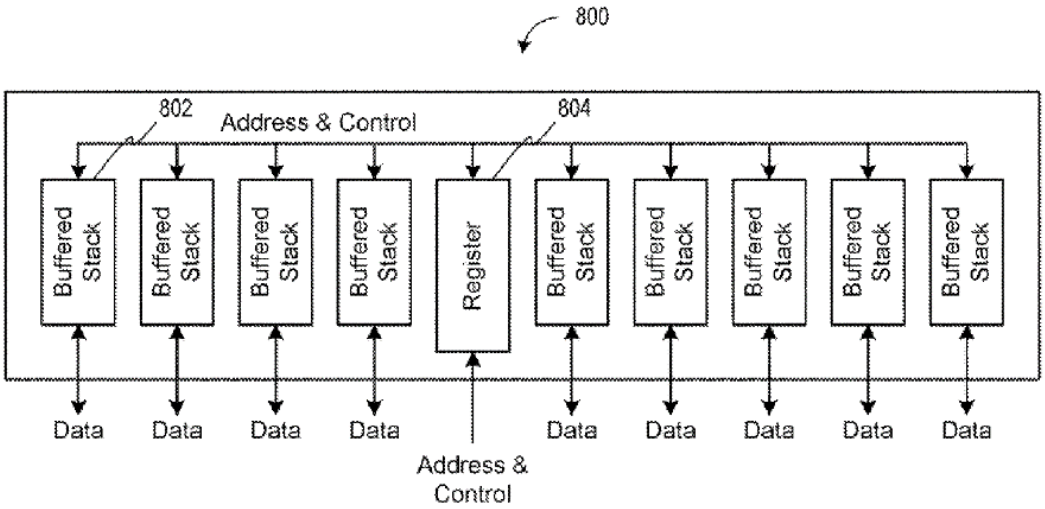


FIG. 8

c) ***[29.c]-[29.g.4]***

The limitations of claim 29 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 4 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[29.c]	[1.a][13]	¶¶1104-1108 (¶¶706-710)
[29.d.1]	[1.b]	¶¶1109-1112 (¶¶711-718)
[29.d.2]	[1.b]	¶¶1113-1116 (¶¶711-718)
[29.e]	[1.c]	¶¶1117-1120 (¶¶719-726)
[29.f]	[1.d.1]-[1.d.2]	¶¶1121-1124 (¶¶727-744)
[29.g.1]	[1.e.1]	¶¶1125-1129 (¶¶745-752)
[29.g.2]	[1.e.2]-[1.e.3]	¶¶1130-1133 (¶¶753-769)
[29.g.3]	[4.a]-[4.b], [6.a]-[6.b][14]	¶¶1134-1137 (¶¶799-810, 817-832)
[29.g.4]	[11.e.5]	¶¶1138-1141 (¶¶919-928)

17. Claim 30

Ground 4 teaches "*[t]he memory module of claim 29, wherein the register device* [from [29.b] (p.134)] *is further configured to perform rank multiplication by generating the chip select signals* [see pp.8-11 (rank multiplication); EX1015, 3:27-30, 6:30-7:67, 8:56-58 ("In one embodiment the emulation is performed at the

[13] See also note 4 on p.77.

[14] E.g., the array dies' received chip-select signals are buffered or generated from the control die's received chip-select signals. EX1003, ¶1137; *supra* pp.8-11, 112-115, 116-119.

DIMM level.")], *and wherein the control signals include the chip select signals* [from [29.d.2] and [29.g.3] above]." EX1003, ¶¶1142-1149.

18. Claim 31

Ground 4 teaches "*[t]he memory module of claim 29, wherein the control signals include data path control signals* [see claim 2 (pp.108-109), e.g., chip select signals] *generated by the register device* [see claim 30 (p.135); *see also* claim [29.b] (p.134)], *the data path control signals being used to control the respective states of the first data conduit and the second data conduit* [see claim [1.e.4] (pp.106-108) and claim 2 (pp.108-109); *see also* claim [29.g.4] (p.135)]." EX1003, ¶¶1150-1158.

19. Claim 32

Ground 4 teaches "*[t]he memory module of claim 29, wherein the control die* [from [29.g.1] (p.135)] *is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal* [see pp.8-11 (rank multiplication); claim 16 (p.132); EX1015, 3:27-30, 6:30-7:67, Fig.18]." EX1003, ¶¶1159-1168.

20. Claim 33

Ground 4 teaches "*[t]he memory module of claim 29, wherein the control signals include command/address signals* [see claim [4.a] (pp.112-114)], *and the control die is configured to hold the command/address signals to control timing of the command/address signals* [e.g., Rajan's buffer chip receives command/address

signals for a write command and holds those signals for "an extra two clocks of delay" to control the timing of when the stacked DRAMs receive those signals, EX1015, 9:46-10:27, Fig.11 (below)]." EX1003, ¶¶1169-1176. A POSITA would have been motivated by Rajan's teachings to implement this command/address signal delay in Riho's device to emulate the characteristics of JEDEC-standard memory devices, including timing. EX1015, 9:46-10:4; EX1019, pp.23-24 ("CAS latency"); EX1003, ¶1174.

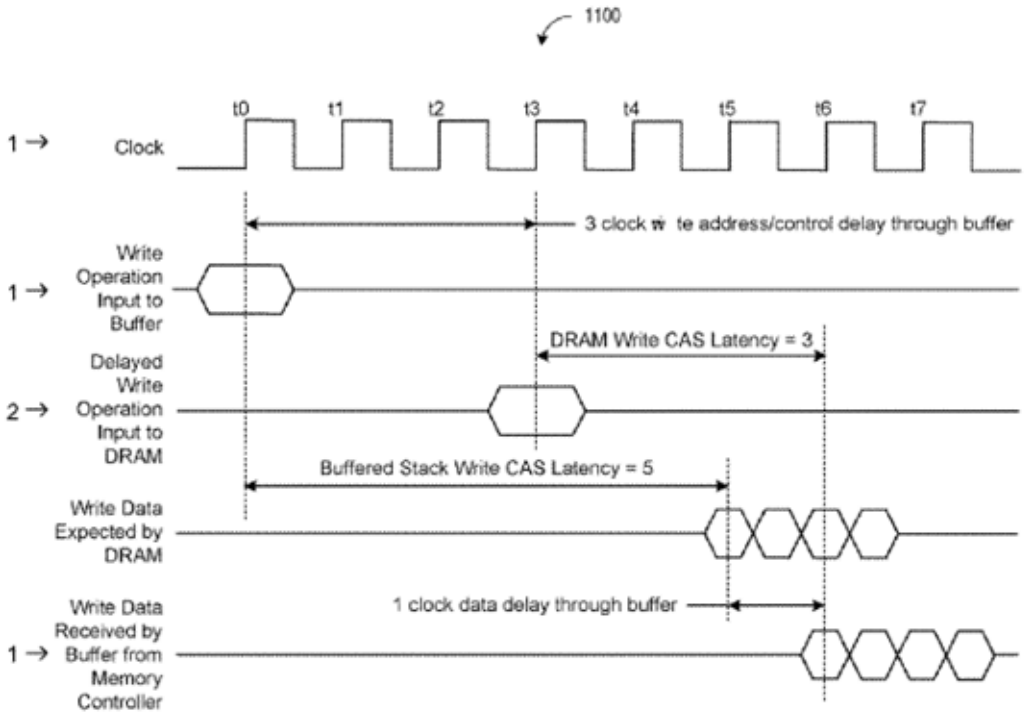


FIG. 11

21. Claim 34

Ground 4 teaches "*[t]he memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the*

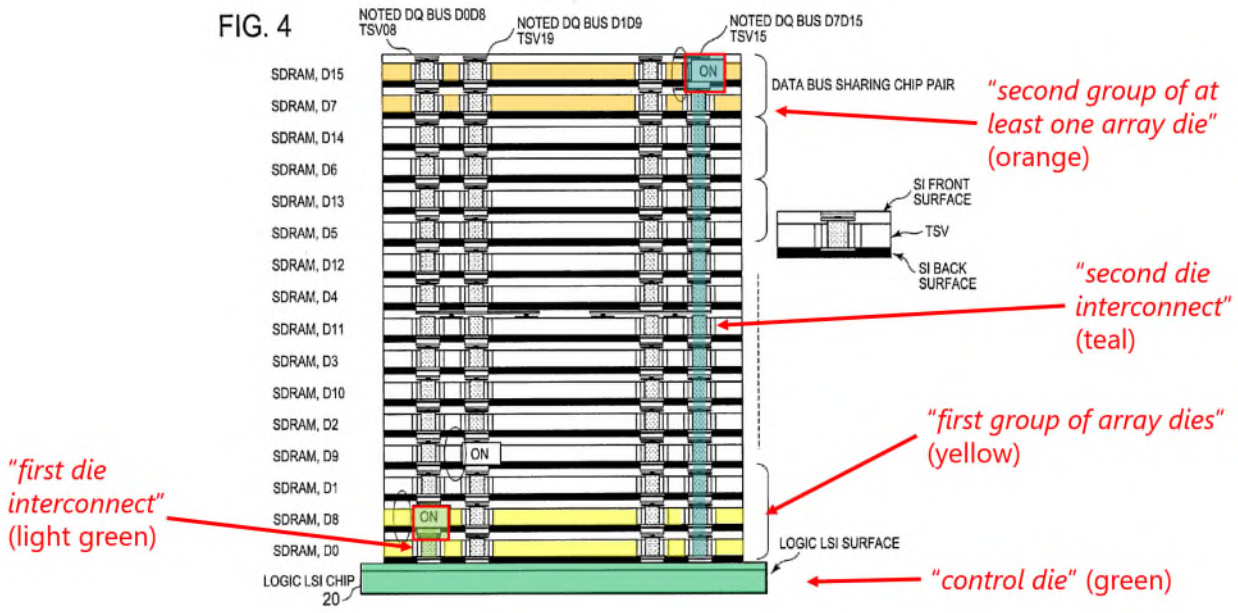
control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit," as explained for [1.e.4] (pp.106-108) and claim 3 (pp.109-111). EX1003, ¶¶1177-1181.

E. Ground 5 (Ground 4 + claims 15, 20-28)

1. Ground 5 combination: Ground 4 and Riho2 (EX1018)

Ground 5 combines Ground 4 (Riho with Rajan) with Riho2 (EX1018). EX1003, ¶¶693-703. Ground 5 thus renders obvious the same claims as Ground 4, plus claims 15 and 20-28 as discussed below.

Riho2 is analogous art to Riho (shown below) and the 060 Patent since each is directed to improving communications between stacked chips. EX1018, ¶¶[0003, 0010], Fig.7A; EX1016, ¶¶[0002, 0012], Fig.4 (below); EX1001, 1:18-21, 5:23-26; EX1003, ¶¶695-700.



Riho2 discloses a circuit (below) for optimizing output drive capacity "according to a change in the time constant caused by parasitic capacitance and parasitic resistance." EX1018, ¶¶[0003, 0010, 0097], Fig.7A (below).

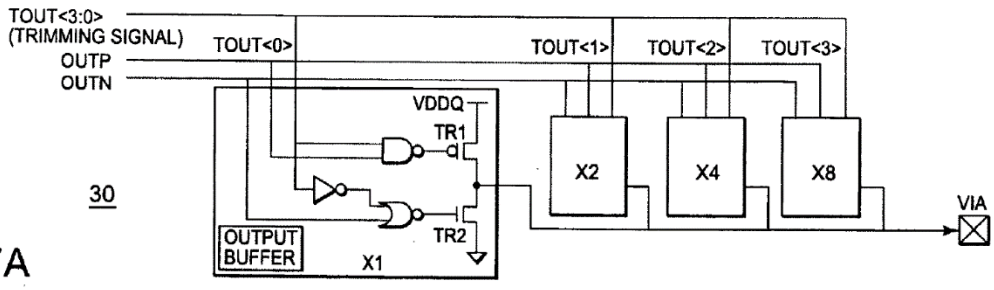


FIG. 7A

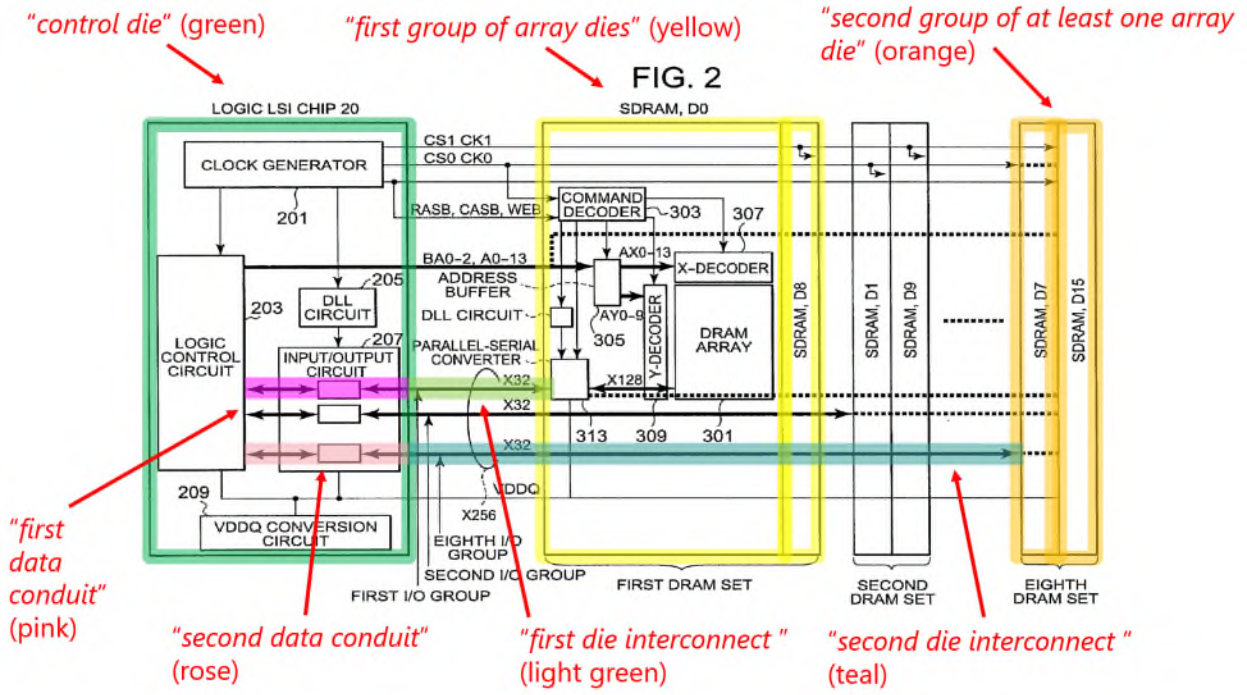
A POSITA would have been motivated to combine Riho and Riho2 for at least two reasons. First, as explained above, they are closely related references with the same inventor, so a POSITA would naturally look to Riho2 for additional details about implementing Riho. EX1003, ¶¶700-701. Second, Riho discloses that impedance and resistance may vary due to variations in the TSVs and distance of the SDRAM chip, *see, e.g.*, EX1016, ¶¶[0055-56, 0061], and Riho2 teaches how to optimize the drive capacity of the output buffers in the control chip to account for these variations, *see, e.g.*, EX1018, ¶¶[0096-97], Fig.7A (above); EX1003, ¶¶696-699. A POSITA would be motivated to use the techniques of Riho2 to improve efficiency, and the combination would be well within the skill of a POSITA and provide the predictable result of conserving power when driving signals through Riho's TSVs. EX1003, ¶¶701-703; *see also* EX1017, 1:22-24

(utilizing the full capacity of a driver for stacked chips would be "wasteful and inefficient"), 5:11-14, Fig.5; EX1039, Abstract, 7:46-49, Fig.6.

2. Claim 15

a) ***[15.a] First and Second Data Conduit***

Ground 5 teaches "*[t]he memory package of claim 11, wherein: the first data conduit* [(pink, below)] *comprises at least a first driver having a first driver size, and the second data conduit* [(rose, below)] *comprises at least a second driver having a second driver size, and*," EX1003, ¶¶950-962.



Drivers were well-known (pp.6-8), and it would be obvious to a POSITA from Riho's disclosure that "[e]ach input/output circuit 207 sends and receives 32-bit width data signals DQ between itself and the SDRAMs D0 to D15 …. [using] interface circuits such as buffers" to use "*driver[s]*" in the "*data conduit[s]*" to

produce enough current to transmit the data signals from one chip ("*control die*") to another chip ("*array die*"). EX1016, ¶¶[0040, 0045-46]; EX1030, pp.135-36 ("buffers are…used when high current flow is needed to drive external devices"); EX1038, p.68 ("tri-state drivers" are "commonly used"); EX1003, ¶953.

Furthermore, as described above (pp.138-140), a POSITA would have been motivated by Riho2 to optimize the drive capacity of each "*data conduit*" to account for manufacturing variations in the TSVs, including impedances, and different positions of the SDRAM chips, as taught by Riho. EX1016, ¶¶[0055-56, 0061]; EX1018, ¶¶[0096-97], Fig.7A (below); EX1017, 1:22-24, 5:11-14, Fig.5; EX1039, Abstract, 7:46-49, Fig.6; EX1003, ¶¶954-960.

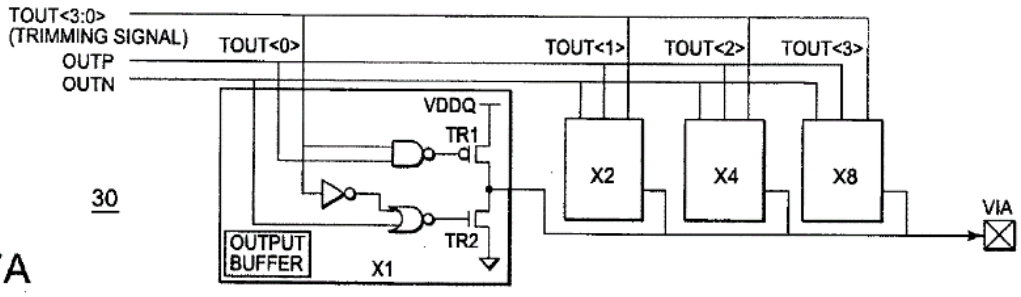


FIG. 7A

b) ***[15.b] Driver Size***

Ground 5 teaches "*wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation*" given Riho's technique of dividing the SDRAMs into groups to reduce the load by half, EX1016, ¶¶[0013, 0103, 119-20], and given

Riho2's technique to optimize the driver size according to the load, *see supra* pp.6-8, 138-140; EX1018, ¶[0097], Fig.7A; EX1017, 1:45-47, 6:44-50; EX1003, ¶¶963-971.

3. Claims 20-28

The limitations of claims 20-28 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 5 for at least the same reasons discussed above:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[20.a]	[1.a][15]	¶¶1000-1003 (¶¶706-710)
[20.b.1]	[1.c]	¶¶1004-1007 (¶¶719-726)
[20.b.2]	[1.d.1]-[1.d.2]	¶¶1008-1011 (¶¶727-744)
[20.b.3]	[1.e.1]	¶¶1012-1015 (¶¶745-752)
[20.b.4]	[1.b]	¶¶1016-1019 (¶¶711-718)
[20.c]	[20.a]	¶¶1020-1023 (¶¶1000-1003)
[20.d.1]	[1.b], [1.e.2]-[1.e.3]	¶¶1024-1027 (¶¶711-718, 753-769)
[20.d.2]	[1.b], [1.e.4]	¶¶1028-1031 (¶¶711-718, 770-778)
[20.d.3]	[4.a]-[4.b], [6.a]-[6.b][16]	¶¶1032-1035 (¶¶799-810, 817-832)

[15] See note 6 on p.89.

[16] See note 14 on p.135.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[20.d.4]	[11.e.5], [15.a]	¶¶1036-1039 (¶¶919-928, 950-962)
[20.e.1]-[20.e.2]	[1.d.1]-[1.d.2]	¶¶1040-1043 (¶¶727-744)
[21]	[15.a]-[15.b][17]	¶¶1044-1048 (¶¶950-971)
[22]	[15.b]	¶¶1049-1053 (¶¶963-971)
[23]	[16]	¶¶1054-1058 (¶¶972-979)
[24]	[4.a]-[4.b][18]	¶¶1059-1063 (¶¶800-810)
[25]	[5]	¶¶1064-1068 (¶¶811-816)
[26]	[12][19]	¶¶1069-1073 (¶¶929-935)
[27.a]	[3]	¶¶1075-1078 (¶¶787-798)
[27.b]	[3], [11.e.5], [15.a]	¶¶1079-1082 (¶¶787-798, 919-928, 950-962)
[28]	[3], [11.e.5], [15.a]	¶¶1083-1087 (¶¶787-798, 919-928, 950-962)

[17] The Riho-Riho2 combination teaches that a driver size is selected based on load, e.g., parasitic capacitance and resistance. EX1018, ¶[0097]; EX1003, ¶1048.

[18] See note 9 on p.90.

[19] See note 10 on p.91.

VIII. §325(d)

Advanced Bionics and §325(d) do not support discretionary denial. The Examiner never considered the references asserted here (Kim, Rajan, Riho, Wyman, Riho2). Although the Examiner discussed a different reference (Rajan137) with the same inventors as Rajan (as discussed above, p.15), the Examiner did not consider Rajan or Rajan137 in combination with the other references in Grounds 1-5 discussed above. Denial under §325(d) is thus unwarranted. *E.g.*, *Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18, at 8-9 (PTAB Aug. 12, 2021). Furthermore, the combinations of Grounds 1-5 clearly render obvious the limitations that Patent Owner contended were missing from Rajan137 (discussed above, p.15), including a plurality of stacked "*array dies*," and a "*first*" and "*second*" "*data conduit*" in the control die, as discussed in the limitation-by-limitation analyses above.

IX. *FINTIV*

The *Fintiv* factors and the Interim *Fintiv* Guidance (EX1047) favor institution. There is one case currently pending between the parties involving the 060 Patent, filed in the Eastern District of Texas, which was amended in May 2022 to add the 060 Patent. EX1043-45. This petition was filed quickly, within 3 months, and the litigation with respect to the 060 Patent is just getting started. As shown above, the merits of this petition are compelling. Thus the *Fintiv* factors

favor institution. EX1047, pp.3, 8-9; EX1048, p.35; *Samsung Elecs. Co. v. Staton Techiya, LLC*, IPR2022-00324, Paper 13, at 12 (PTAB July 11, 2022) ("24.2 months"); *Siemens Indus. Inc. v. EMA Electromechanics, Inc.*, IPR2021-01517, Paper 9, at 11-12 (PTAB Mar. 15, 2022) (factor 2 neutral when FWD deadline less than one month after potential trial date).

X. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-34 be canceled as unpatentable.

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24 because it contains 13,910 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 26th day of August, 2022, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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